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PHOTOVOLTAIC DEVICES ON CdS AND $Zn_xCd_{1-x}S$ SINGLE CRYSTALS

by

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A thesis submitted in accordance with the regulations for the degree of Doctor of Philosophy in the University of Durham

1982

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CONTENTS

ABSTRACT

Photovoltaic devices have gained considerable importance in recent years as a possible alternative solution to the energy problem. The main criterion for these devices for power generation on a large scale is that they must make a positive contribution to the energy balance. With the present level of research and development, CdS and $Zn_xCd_{1-x}S$ based thin film solar cells have emerged as the main contenders in the near future for large scale terrestrial solar energy conversion. However, the many problems with these thin film photovoltaic cells are not yet well understood, although a great deal of effort has been put into their research and development since 1960. In order to avoid the complications associated with polycrystallinity, grain boundaries and other thin film defects, the work reported in this thesis has been carried out on oriented single crystal substrates.

The first part of the thesis describes an investigation into CdS/Cu_2S devices. This includes the major processes involved in the fabrication of these cells and the determination of the effects variations in these processes have on the electronic and optoelectronic properties of the completed devices. By using the techniques of scanning electron microscopy and reflection electron diffraction in conjunction with conventional electrical and photoelectrical measurement techniques, it has been established that there is a direct correlation between the overall surface topography and resultant device characteristics. Further specific surface features such as ledges and kink sites on etch hillocks are directly associated with the loss of local photovoltaic sensitivity. The chemiplating process by which the surface layer of CdS is converted into copper sulphide has been improved by introducing three modifications, which enable the chalcocite phase of the copper sulphide to be produced in a much more controlled manner. The effect of a post barrier

air-bake has also been investigated. It is shown that this treatment is only beneficial for cells which have poor operational parameters in their as-prepared condition. However, for cells with good characteristics at this stage, there is no advantage to be gained from the air-bake. In fact this process has undesirable features causing degradation in the performance of these cells. The investigation of minority carrier diffusion lengths revealed that they are independent of surface preparation and post barrier air-baking in Cu_xS whilst in CdS they are strongly affected by variations at these two fabrication stages. Dark current conduction processes in CdS/Cu_2S heterojunctions have also been analysed, and are shown to be governed by thermally activated tunnelling and recombination. A multi-diode model is suggested together with a potential energy diagram of the heterojunction barriers.

The second part of this thesis is concerned with $Zn_xCd_{1-x}S$ single crystals and devices prepared on them. Similar studies to those on CdS/Cu_2S heterojunctions were made. It has been demonstrated that both the lattice parameters (a_o, c_o) of $Zn_xCd_{1-x}S$ mixed single crystals decrease sublinearly with increasing zinc composition. The properties of the photovoltaic cells prepared on $Zn_xCd_{1-x}S$ single crystals are closely related to those of devices fabricated on CdS substrates. The open circuit voltage obtained under 100 mW cm^{-2} (AM1) illumination increased with zinc content to 0.72 V with a $Zn_{0.4}Cd_{0.6}S$ based cell, but simultaneously there was a considerable decrease in the short circuit current. One difficulty is that proportions of copper deficient phases in the copper sulphide layer increased with rising zinc content in the substrate.

ACKNOWLEDGEMENTS

I would like to express my appreciation for the valuable guidance and helpful encouragement given by my supervisor, Dr. J. Woods. I am also indebted to Dr.G. J. Russell for many constructive discussions and suggestions as well as his instructions and help in the use of the transmission and scanning electron microscopes during the course of this work.

I would also like to thank Professor G.G. Roberts for allowing me to use the facilities of the Department of Applied Physics and Electronics, University of Durham, and I am grateful to members of the workshop, headed by Mr.F. Spence, for their willingness to provide their skill and advice.

I wish to extend my thanks to Mr.N.F. Thompson both for his technical assistance in the laboratory and in the crystal growth and also for the drawing of the diagrams used in this thesis. Further, I would like to express my gratitude to Mrs.S. Mellanby for her advice and patience whilst typing this thesis. In addition, special thanks are due to Mrs. D.Williamson and to several friends for checking the language and grammar in this thesis.

My appreciation is also extended to the Turkish Ministry of National Education for an award of a research studentship and for providing financial support over three years.

Finally, I am particularly indebted to my parents for their many sacrifices and constant encouragement over the years, and to my wife, Nurgün, for her understanding, patience and support.

CHAPTER 1

INTRODUCTION TO PHOTOVOLTAIC CELLS

1.1 INTRODUCTION

The direct conversion of sunlight into useful electricity, in the form of a D.C. voltage and current, by a photovoltaic device (or solar cell) has the potential of providing significant usable energy from the sun's inexhaustible supply. The photovoltaic effect, discovered over a hundred years ago, is the creation of an electromotive force (EMF) by the absorption of light in an inhomogeneous solid or device,and is different from the production of an EMF by the thermo-electric effect (i.e. localized heating), or by the Dember effect[1] which results from non-uniform illumination in homogeneous samples.

In order to produce a photovoltaic effect in a system, the radiation must generate charge carriers, both electrons and holes, which must be separated by an internal electric field created by some electronic inhomogeneity in the device (i.e. p-n junction, metal-semiconductor, or metal-insulator semiconductor junction). In addition the carriers generated must be able to travel in their separated state up to the boundary of the internal electric field. The processes of creation and diffusion of charge carriers are associated with the current generation aspects, while the internal field is the determining factor for the voltage and current.

The history of the photovoltaic effect originated with Becquerel (1839)[2], who studied metal electrodes immersed in a liquid electrolyte and observed that the current between two electrodes changed considerably when one electrode was illuminated. Adam and Day[3] observed a similar effect using platinum contacts on selenium, in 1877. Thereafter up to the early 1950's a variety of materials and devices had been investigated in order to convert sunlight into electricity, but the best efficiency was less than 4%.

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In 1954 Reynolds et al[4] reported the observation of the photovoltaic effect in cadmium sulphide single crystals. This work led to the development of the CdS/Cu_2S thin film photovoltaic cell during the early 1960's[5,6]. Also, in 1954, Chapin, Fuller and Pearson[7] reported 6% efficiency for p-n junction devices on single crystal silicon. The first analytical treatment of solar cell efficiency was published in 1955 by Prince[8], and Loferski[9] suggested that the optimum energy gap for a p-n junction solar cell should be 1.5 eV. In recent years many groups have fabricated solar cells using a large variety of material and techniques and the highest efficiency reported to date is 24.7% which was achieved with GaAs based cells[10].

1.2 MATERIALS FOR PHOTOVOLTAIC APPLICATIONS

Critical issues in the selection of materials for solar applications are the performance, cost, life and availability. A solar cell can be considered to consist of two parts,namely an absorber and a collector. The factors affecting the choice of absorber materials are : the energy gap, the absorption coefficient and minority carrier diffusion length. In order to achieve 90% of the maximum possible output from the diode, the energy gap of the absorber should be between 1.0 and 1.7 eV, and the diffusion length two times that thickness required to absorb 90 percent of the incident photons[11]. The other important parameters required for the absorber are the optimal resistivity to minimise the power losses and the stability to perform within specifications during its lifetime. The second important part of a solar cell is the collector, which collects the generated minority carriers and converts them into majority carriers at the maximum voltage, limited by the excitation energy of the generated minority carriers. With heterojunction photovoltaic devices, the desirable characteristics are ; a reasonable electron affinity and good lattice matching between the absorber and the collector, together with a high mobility in the collector for converted carriers. If the electron affinity of the collector is greater than

that of the absorber a negative discontinuity in the conduction bands appears with a consequent reduction in the achievable open circuit voltage. In contrast, if the absorber has a higher electron affinity than that of the converter, a spike (a positive discontinuity) occurs in the conduction band at the interface and this gives rise to a reduction in the short circuit current. Any mismatch between the lattices of the absorber and the collector leads to a high density of interface states which causes the generated carriers to recombine at the interface before they can be collected. Thus the lattice match between materials is one of the important requirements in the choice of photovoltaic materials. More detailed discussion on the properties of materials for solar cells can be found in Ref (12).

1.3 CLASSIFICATION OF PHOTOVOLTAIC CELLS

Photovoltaic devices may be categorized into several systems but most commonly they are classified according to their micro and macro-structure, the degree of perfection of the material used,and the type of electronic junction formed. In the first classification there are : (i) single crystal cells ; although these have the highest efficiency,as a consequence of their crystal perfection, they are the most expensive, (ii) polycrystalline cells ; this type of cell includes photovoltaic devices fabricated on evaporated, sputtered, ion beam deposited, sprayed and electrophoretic layers or on bulk material made by casting, sintering, directionally solidifying, silk screen printing and grown by simple melting. Although such cells are not usually expensive to produce, the efficiency and the stability of polycrystalline cells produced to date are still not at the desired level as a consequence of complex difficulties associated with the effects of grain boundaries and defects, (iii) amorphous cells ; amorphous materials are relatively new in photovoltaic applications, but their low cost and promising characteristics make them strong candidates for large scale terrestrial applications.

In the second scheme a photovoltaic device can be designated as (i) a homojunction cell, which consists of regions of the same semiconductor doped n and p-type, (ii) a heterojunction cell, which is composed of two different semiconductors, (iii) a Schottky barrier diode which is a metal-semiconductor junction and (iv) a metal-insulator-semiconductor (MIS) cell.

Although there is no problem of matching lattices and electron affinities with homojunctions, they are obviously limited to materials which can be made both n- and p-type. In contrast heterojunction photovoltaic cells can be fabricated from a large variety of pairs of semiconductors. The disadvantages with heterojunctions are that there are inevitable interface complexities and band discontinuities associated with the mismatch of two materials. Indeed, it is often easier and cheaper to produce Schottky barrier photovoltaic devices, but the resultant efficiency is usually limited to low values. This limitation can be overcome by using an insulating layer between the metal and the semiconductor.

1.4 DEVELOPMENT OF PHOTOVOLTAIC CONVERSION AND ECONOMIC ASPECTS

Although photovoltaic devices have gained considerable importance in recent years as a possible alternative solution to the energy problem, single crystal silicon solar cells are still the only ones widely used and commercially available. However, such cells are expensive to make both in terms of money and energy consumption, and they are limited in area. Of the possible alternative thin film cells which would be cheap and large area, CdS/Cu_2S, $Zn_xCd_{1-x}S/Cu_2S$ and amorphous silicon have emerged as the main contenders. As research and development on amorphous silicon is fairly recent, cells based on CdS and $Zn_xCd_{1-x}S$ are at the moment the more serious candidates for large scale terrestrial photovoltaic solar energy conversion.

Although a great deal of effort has been put into the research and development of CdS/Cu_2S thin film solar cells since 1960, progress has been slow and only a limited number of investigators have reported efficiencies

higher than 7%. More recently the Institute of Energy Conversion (IEC) has achieved an efficiency of 9.15%[13]. With the present technology, the efficiency of CdS/Cu_2S thin film photovoltaic cells is estimated to be limited to about 10%[11] mainly because of differences in the electron affinities and the lattice mismatch of the two semiconductors from which the heterojunction is formed. A dramatic improvement in efficiency is expected if the lattice match and the match in the electron affinities can be improved. One way of accomplishing this is to incorporate some zinc into the CdS to form a solid solution of $Zn_xCd_{1-x}S$, as first suggested by Palz et al[14]. Indeed, thin film cells based on $Zn_xCd_{1-x}S$ have recently been produced with an efficiency of up to 10.2%[15]. This is far from the limit for these devices which is estimated to be about 15%[11]. However, since the developing countries represent one of the largest markets for solar cells where the limitations of available land area are far less stringent, reliability and cost can be more important considerations than efficiency. Thus companies are already marketing cells based on CdS which have a guaranteed efficiency of only 3% (Photon Power Inc). During the 3rd E.C. Photovoltaic Energy Solar Energy Conference a group from the University of Stuttgart (W.Germany)[16] reported the achievement of an average efficiency of 7.3% in 2000X 42 cm^2 evaporated front wall CdS/Cu_2S cells. At the same conference, Photon Power Inc (U.S.A.) announced the semi-automated pilot production line which had been installed at El-Paso,Texas to manufacture up to 185000 m^2 per year of CdS/Cu_2S cells at a cost of $2/Wp.

In a field which is developing very fast, it is extremely difficult to be precise about the manufacturing cost of different cells, indeed there is very little published data on the comparison of the economic aspects of different solar cells. The main criterion for solar cells for power generation on a large scale is that they must make a positive contribution to the energy balance (i.e. they should produce more energy during their lifetime than is

consumed during their production). Recently Hay et al[17] compared the energy consumption in fabricating four different types of cell encapsulated in to panels (see Fig 1.1). They have also listed the commodity requirements for the different cells to produce £1. worth of electricity (see Table 1.1). By comparing Fig 1.1 and Table 1.1, it is apparent that the CdS/Cu_2S cell consumes less energy during its preparation than any of the others. Barnet and Rothwarf[11] predicted that IEC's research and development programme will be leading to CdS and $Zn_xCd_{1-x}S$ cells with a manufactured cost of less than $ 0.2/Wp as early as 1986 and less than $0.15/Wp as early as 1990.

1.5 SCOPE OF THE PRESENT STUDY

The work reported in this thesis is primarily concerned with the effects changes in the processes involved in the preparation of CdS/Cu_2S and $Zn_xCd_{1-x}S/Cu_2S$ cells have on the electronic and optoelectronic properties of a completed device. The work has been carried out on single crystal substrates in order to avoid the complications associated with polycrystallinity, grain boundaries, and other defects characteristic of thin film substrates. Thus the processes of interest, which include surface preparation, orientation and resistivity of the substrates, surface topography, the formation of copper sulphide layer, heat treatment, etc. have been investigated using the techniques of scanning electron microscopy (SEM) and reflection electron diffraction (RED) in conjunction with conventional electrical and photoelectrical measurements. Chapter 2 provides a general review of the material properties of CdS, $Zn_xCd_{1-x}S$ and Cu_2S, and Chapter 3 contains the theory of heterojunctions, and the conduction mechanisms and models proposed for the CdS/Cu_2S cell. The techniques and apparatus used are described briefly in Chapter 4.

The results obtained can be divided into two parts : The first part consists of Chapters 5, 6, and 7 and describes the work on CdS/Cu_2S devices. The results presented are concerned with surface preparation prior to the formation of the copper sulphide, the chemiplating process and its optimization, the study of the structural phases and thickness of the copper sulphide and

Figure 1.1 : Energy content of four different types of solar cell (Ref.17).

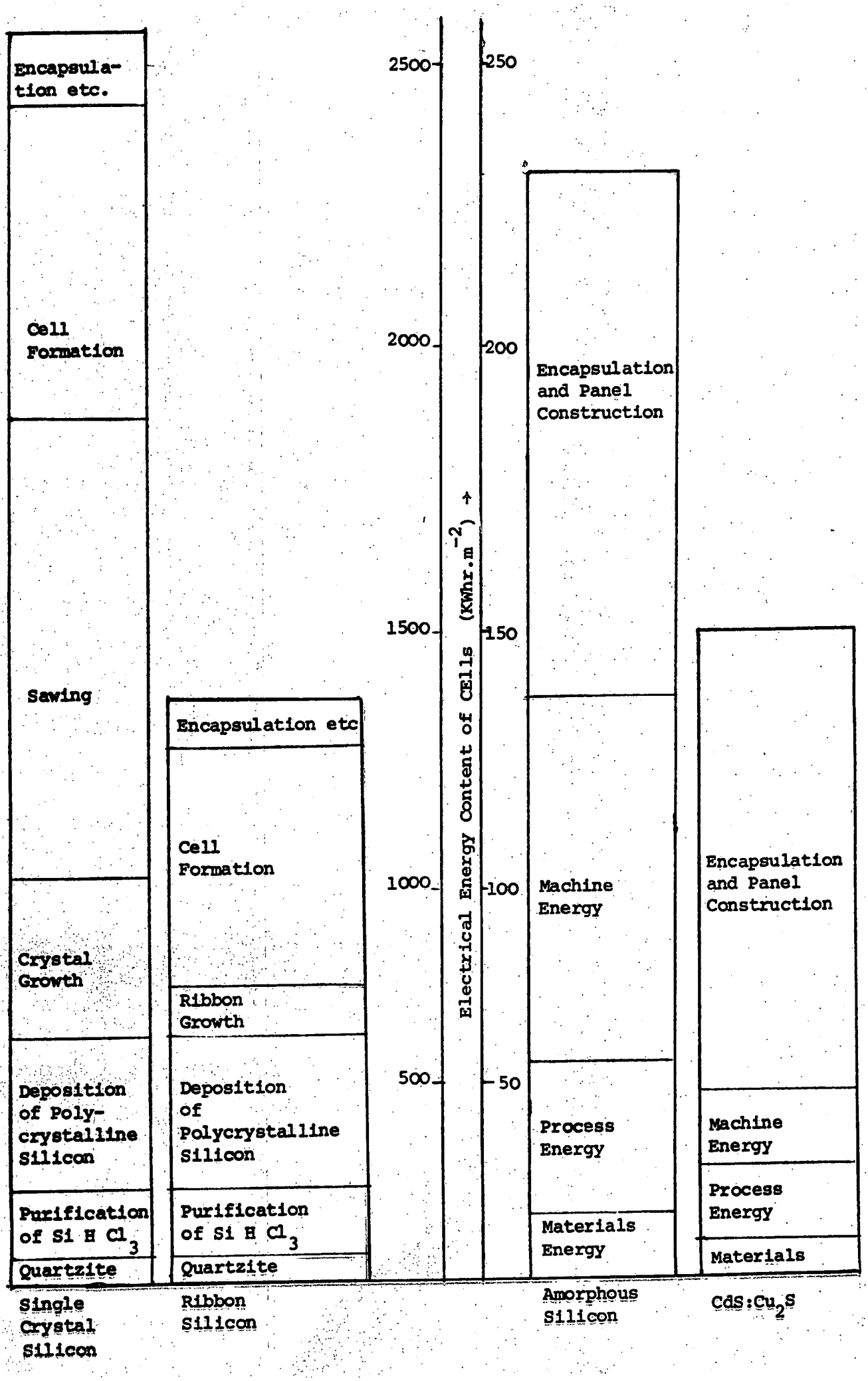

TABLE 1.1 : Commodity requirements (in pence Sterling) to be bought in by the solar cell industry to produce £1 worth of solar cell generated electricity (commodities worth less than 0.1 pence not shown) (Ref.17).

U.K.Department of Industry Classification	Type of Cell			
	Crystalline Silicon (Cz.process)	Amorphous Silicon	Sputtered and Thermally deposited CdS : Cu_2S	Sprayed CdS : Cu_2S
Chemicals	-	-	0.6	-
Other Iron and Steel	1.2	2.2	1.3	1.9
Aluminium and Aluminium Scrap	1.6	1.6	1.6	1.6
Other non-ferrous metals	1.7	6.8	4.9	6.1
Building materials	3.2	0.1	0.2	0.1
Timber and furniture	0.1	-	-	-
Man-made fibres	0.2	0.6	0.8	0.9
Other Manufacturing	1.6	0.6	0.3	0.6

the effect that changes in these parameters have on the device characteristics. The effects of baking devices in air at 200°C were also investigated. By using the electron beam induced current mode in the SEM, localized variations in the efficiency have been correlated with topographical features. The minority carrier diffusion lengths in CdS and Cu_2S have also been determined. Finally, the mechanism of dark current conduction has been studied and the capacitance voltage characteristics of the junctions are also reported. A band structure model is proposed to explain the results.

The second part of the work is described in Chapter 8, where the results on $Zn_xCd_{1-x}S$ single crystals and the heterojunctions prepared on them are reported. These studies are similar to those made on CdS/Cu_2S devices. They include an investigation into the growth and characterization of $Zn_xCd_{1-x}S$ single crystals, surface preparation before chemiplating, the properties of the converted copper sulphide layer and the characteristics of heterojunction devices formed on these substrates.

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CHAPTER 2

MATERIALS ASPECTS OF CdS, (Cd Zn)S AND Cu_xS FOR SOLAR CELL APPLICATIONS

2.1 INTRODUCTION

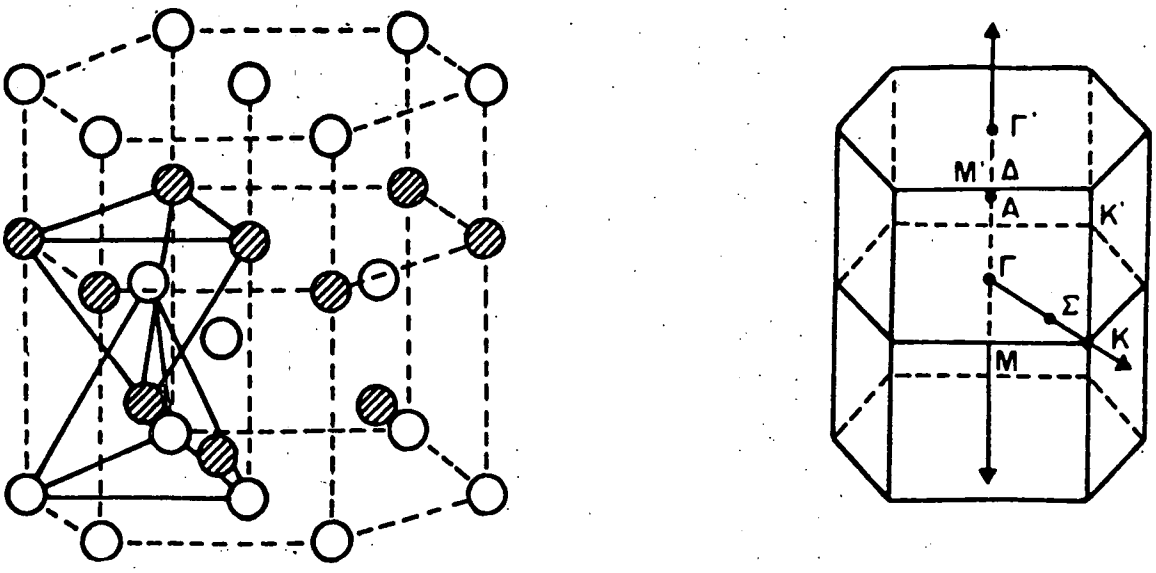
It is the intention in this chapter to focus on the materials aspects of cadmium sulphide, cadmium sulphide-zinc sulphide solid solutions and copper sulphide for solar cell applications. The optical and electronic properties and structural aspects of these materials will be discussed.

A general review of the well established properties of CdS is given in section 2.2. The comparison of CdS with ZnS is followed by a survey of the (CdZn)S alloys in section 2.3. The copper sulphide layer plays a very important role in this type of photovoltaic cell. The relatively complicated properties exhibited in numerous copper sulphide phases are summarised and discussed in section 2.4.

2.2 FUNDAMENTAL PROPERTIES OF CADMIUM SULPHIDE

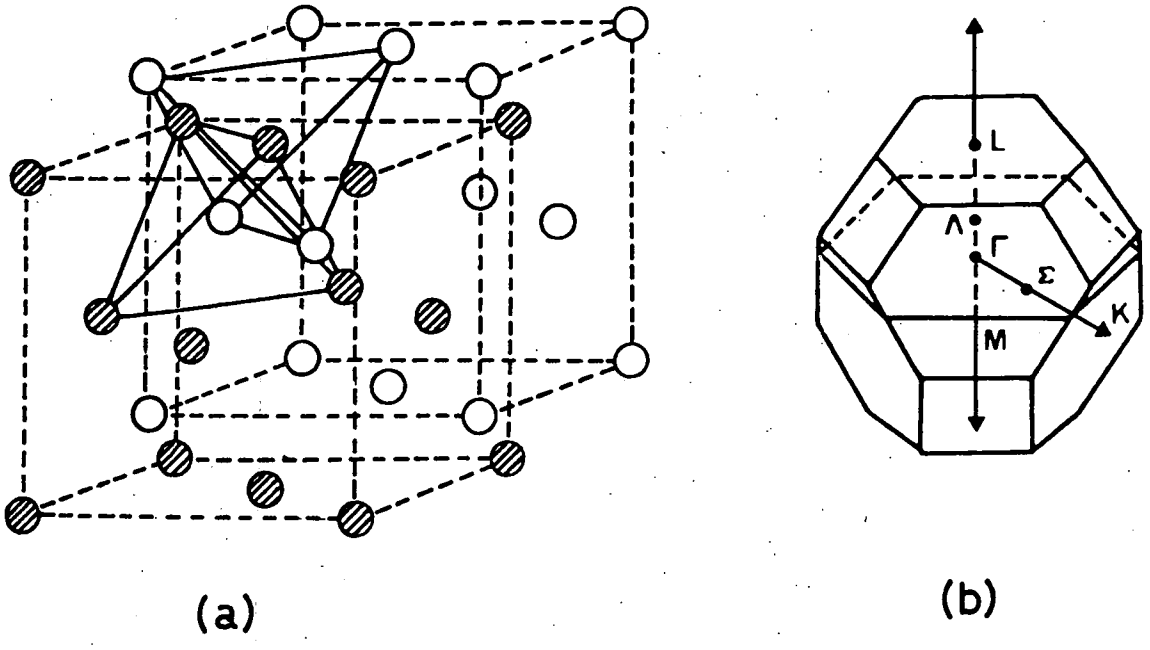
The compounds formed between elements from group II and VI of the periodic table are called II-VI compounds. CdS is one of these. It is a semi-insulating compound which crystallizes in two allotropic forms with the wurtzite and zincblende structures. The wurtzite structure consists of two interpenetrating hexagonal lattices displaced with respect to each other by a distance of $3c/8$ along the c-axis, (Fig 2.1a). The nearest neighbour distance in the wurtzite structure with ideal tetrahedral sites is $3c/8$ or $(3/8)^{\frac{1}{2}}a$ which gives a (c/a) ratio of $(8/3)^{\frac{1}{2}} = 1.632$ with $a = 4.613$ Å and $c = 6.716$ Å [1]. The zincblende structure, which is in the cubic crystal class, is composed of two interpenetrating face-centred cubic lattices, illustrated in Fig 2.2a, translated with respect to each other by one quarter of the body diagonal. The nearest neighbour separation in this instance is $a\sqrt{3}/4$ with lattice parameter $a = 5.832$ Å [1].

The wurtzite and zincblende structures are both characterised by tetrahedral lattice sites (Fig 2.1a and Fig 2.2a) and as a consequence



(a) (b)

FIG. 2·1 (a) WURTZITE STRUCTURE ILLUSTRATING TETRAHEDRAL SITE
(b) DOUBLE BRILLOUIN ZONE FOR WURTZITE STRUCTURE



(a) (b)

FIG. 2·2 (a) ZINC BLENDE STRUCTURE
(b) BRILLOUIN ZONE FOR ZINC BLENDE

their nearest-neighbour environment is identical, but positional and directional differences exist beyond the next nearest neighbours. The crystal field effect which results from such differences is sufficiently small to permit general comparison of energy bands in wurtzite and zinc-blende structures[2]. The changes in band structure can be simply discussed in terms of two Brillouin zones, i.e. the first Brillouin zone of zincblende structure is the same as that of elemental diamond (a truncated octahedron), whereas the double zone scheme must be used for the wurtzite structure as twice as many atoms exist in a unit cell. For a detailed discussion see references 1 and 3.

The band structure of CdS has been studied thoroughly,[4,5,6,7], and it is concluded that the maximum of the valence band and the minimum of the conduction band are situated at the centre of the Brillouin zone, $a\underline{k} = 0$. The lowest conduction band is associated with the cadmium 5s levels and the highest valence band with the sulphur 3p levels[5]. The conduction and valence band structure for wurtzite crystals around $\underline{k} = 0$ is shown in Fig 2.3. CdS is a direct-gap semiconductor, which means that the optical absorption coefficient changes as the square of the incident photon energy and has a very large magnitude for photon energies just greater than the bandgap. The temperature bandgap relation obtained from optical reflection and transmission measurements is

$$Eg = 2.58 - (5.2 \times 10^{-4})\ T\ (K)\ (eV) \qquad (1)$$

From this equation, the bandgap turns out to be 2.42 eV at room temperature. Some other parameters of CdS are listed in Table 1.

As-grown CdS contains cadmium vacancies, sulphur vacancies, cadmium interstitials and associated complexes of these defects. It has a low density of intrinsic carriers, and its conductivity is totally controlled by the presence of native defects and impurities. Cadmium sulphide begins

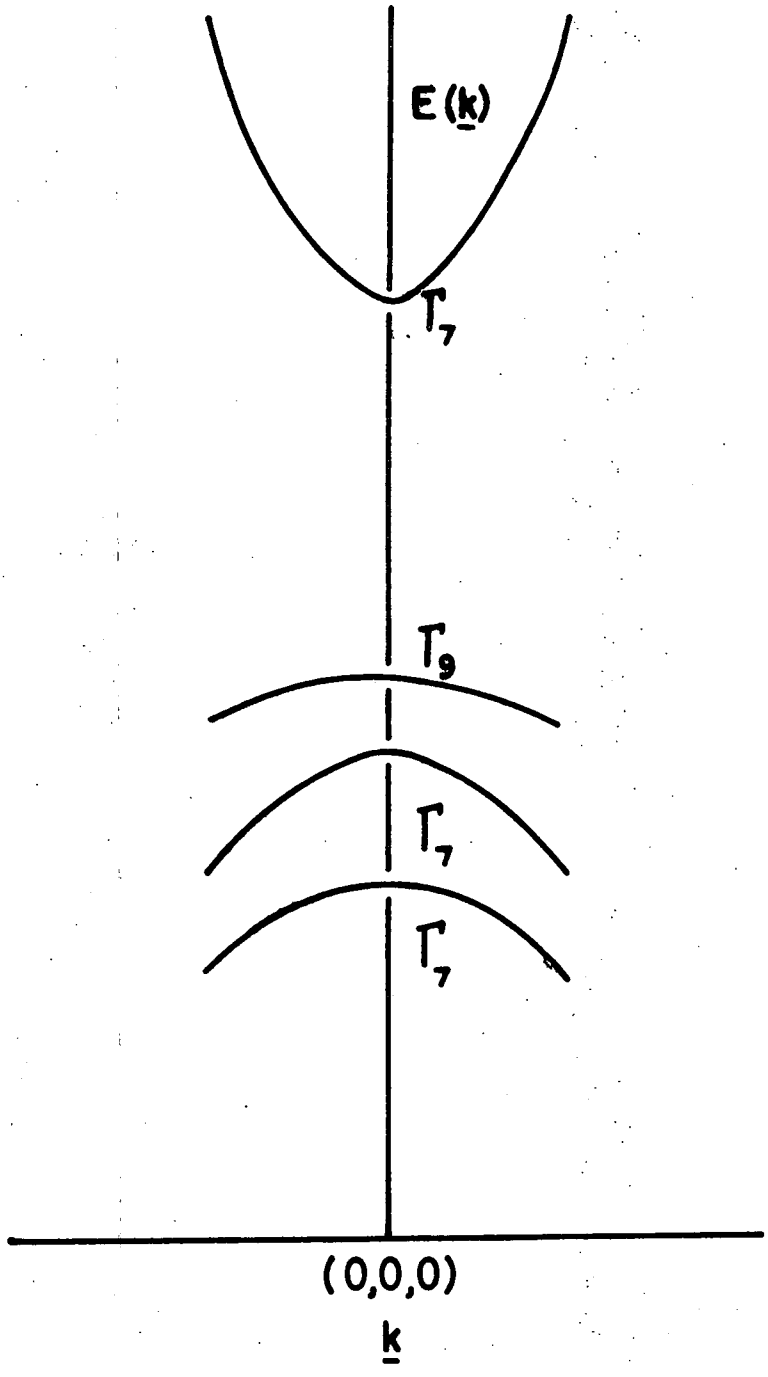


FIG. 2·3 THE CONDUCTION AND VALENCE BAND STRUCTURE FOR WURTZITE CRYSTALS AROUND $\underline{k} = 0$

TABLE 2.1 : Summary of parameters for CdS after Ray (3).

Parameters	CdS (Wurtzite)
Relative density	4.92 gr/cm^3
Molecular weight	144.46
Lattice parameters	a = 4.136 Å b = 6.713 Å
Direct band gap	2.43 eV (300 K)
Effective mass of electrons m^*/m_e	0.153 - 0.171
Effective mass of holes m^*/m_p	0.7 light holes 5.0 heavy holes
Thermal conductibility	0.20 $W\ K^{-1}\ cm^{-1}$ (||C-axis)
Dielectric constant	$\varepsilon \|\| C = 8.64$ $\varepsilon \perp C = 8.28$
Refractive index	2.3 (λ= 2 µm) 2.26 (λ= 14 µm)
Electron mobility	$\sim 400\ cm^2\ V^{-1}\ s^{-1}$
Hole mobility	$15\ cm^2\ V^{-1}\ s^{-1}$

to sublime at about 750°C and melts at about 1750°C, but only under many atmospheric pressures. It is possible to grow single crystals of CdS in a variety of ways, for example such as from the melt under high pressures[8,9], by iodine vapour transport[10] or by direct sublimation from the vapour phase[11]. In fact, the direct vapour phase technique has been developed and used extensively in this laboratory. Only n-type CdS can be produced ; any attempt to incorporate acceptor impurities such as copper or silver results in self compensation by non-metal vacancies. During cooling to room temperature, some of the high temperature vacancy concentration is frozen in. Thus n-type CdS is readily formed by growth under non-stoichiometric conditions in an excess pressure of cadmium vapour (Cd-rich); such crystals may be regarded as self-doped. In fact,of course, the non-stoichiometry can be changed by heating in Cd-or S-vapour, although heating in S-vapour does not produce p-type conductivity. The ratio of the cation radius (r_c) to anion radius (r_a) describes the limitations on the type of conductivity which can be achieved. If $r_c/r_a > 1$, as in most II-VI compounds, then n-type conductivity is possible but not p-type. In contrast, if $r_c/r_a < 1$ p-type conductivity arises, as in ZnTe. For a compound in which $r_c/r_a \simeq 1$, amphoteric conduction occurs (p-type or n-type) as in CdTe. For details see reference (9).

In CdS, substituting chlorine, bromine, or iodine for sulphur, and aluminium, gallium or indium for cadmium creates shallow donor levels 0.03 eV from the conduction band edge. On the other hand, copper and silver produce acceptor levels 0.6 eV and 1.0 eV above the valence band[12]. The alkali metals,sodium potassium and lithium are also acceptor type impurities and produce shallow levels.

Brillson[13,14] has studied the surface properties of CdS and he has concluded that no filled or empty intrinsic surface states can be observed on clean stoichiometric surfaces to an estimated detectability limit of 10^{11} cm^{-2}. He has suggested that the states which do exist on

CdS surfaces are extrinsic in origin. Studies concerning copper diffusion in CdS have special importance for CdS/Cu_xS devices but published diffusion coefficients show considerable spread. A detailed study and discussion can be found in reference (15).

The characterisation of the localised levels introduced into the forbidden gap of pure or intentionally doped CdS samples and their identification with crystal imperfections has been the subject of considerable research[1,12,16], using more or less indirect methods, such as thermally stimulated conductivity, (TSC), photo-decay, space charge limited current (SCLC), spectral photoresponse luminescence, etc (see references 17,18,19). Recently methods such as admittance spectroscopy[20,21], transient capacitance measurements[22], and, after Lang[23], deep level transient spectroscopy (DLTS)[24,25] have been used extensively in the study of carrier trapping properties in CdS. Most recent and detailed data can be found in the paper by Hussein et al[26].

The remarkable photoconductivity, piezoelectric and luminescence properties of CdS and its application as a collector in CdS/Cu_2S solar cells make it one of the most thoroughly investigated II-VI semiconductors.

2.3 PHYSICAL PROPERTIES OF THE CADMIUM SULPHIDE-ZINC SULPHIDE SYSTEM

CdS and ZnS in the wurtzite modification have unit cells with volumes in the ratio $\sim$ 1.26/1 and cation radii with a ratio $Cd^{++}/Zn^{++} \sim 1.3$[1]. The band gaps of the two compounds differ by $\sim$ 1.2 eV ($\sim$ 2.4 eV for CdS and 3.6 eV for ZnS) and with crystals growth by similar methods their extrinsic conductivities are normally many decades apart. However, the band structures CdS and ZnS are not expected to be grossly different[7]. In fact there are a considerable number of qualitative similarities in their photoelectronic properties. For example, they are both n-type photoconductors, they both exhibit analogous edge emission and their reflectivity spectra show similar structures. In addition, native or intrinsic defects play critical roles

in determining the electrical and luminescent properties of both materials. Detailed discussions are given in references 1,3,12. Davis and Lind[27] showed that the growth of (CdZn)S single crystals by iodine vapour transport yields a highly uniform and relatively strain free single crystal of $Zn_xCd_{1-x}S$ with a hexagonal structure. Similar mixed crystal of (CdZn)S have been grown from the vapour phase in this laboratory using a modification of the method described by Clark and Woods[11]. Lattice parameters of (CdZn)S alloys have been studied by Ballentyne and Ray[28] and they showed that the c-axis dimension of the wurtzite structure of alloys decreases sub-linearly with zinc content. Davis and Lind[27] studied the photoelectronic properties of their mixed crystals as a function of composition and concluded that : (1) the dark conductivity of as grown CdS is about 0.1 Ω^{-1} cm^{-1}, incorporating about 15% ZnS into the CdS lattice, decreases this dark conductivity by a little over one order of magnitude. However, with 15-25% zinc the dark resistivity increases by about 7-8 orders of magnitude. From 25% to 60% ZnS, the dark resistivity is about 10^{10} Ω cm and between 60-100 % ZnS a further increase of about 3 orders of magnitude occurs. The photoconductive sensitivity decreases almost linearly by about 5-6 orders of magnitude from CdS to ZnS, (2) the optical band gap of the CdS-ZnS system exhibits a monotonic but non-linear increase with increasing zinc composition, this sublinear variation over the range $\sim$ 2.4-3.6 eV has been confirmed consistently by several workers[28,29,30], (3) a photoconductivity sensitizing level which is almost composition invariant exists throughout the range with an energy of 1 eV above valence band.

There has been great interest in $Zn_xCd_{1-x}S$ alloys, since Palz et al[31] reported that $Zn_xCd_{1-x}S/Cu_2S$ photovoltaic cells offer a significantly higher open-circuit voltage than CdS/Cu_2S junctions. Reported results on devices prepared on polycrystalline, thin-film (CdZn)S alloys[32] agree with those reported in single crystal (CdZn)S. Recently, R.B.Hall et al[33] claimed to have prepared $Zn_xCd_{1-x}S/Cu_xS$ solar cells with 10% efficiency.

This indicates that (CdZn)S based cells are serious candidates for large scale terrestrial photovoltaic solar energy conversion in the near feature.

2.4 PROPERTIES OF COPPER SULPHIDE

In the past few decades, there has been renewed interest in copper sulphide because of its importance in CdS and (CdZn)S solar cells. The primary role of copper sulphide in the heterojunction cell is to act as the photon absorber, thus its properties determine the light generated current. Other considerations are the resistivity of copper sulphide and the lattice match between the copper sulphide and the CdS or (CdZnS). In what follows, bulk properties of copper sulphide such as optical absorption ; electrical resistivity and minority carrier density ; minority carrier lifetime and diffusion length and the lattice structure and spacing, will be reviewed. However, the experimental determination of these properties is relatively complicated by numerous copper-sulphur phases that can exist.

2.4.1 Stoichiometry of the Copper-Sulphur System and Structural Properties of the Various Phases

A phase diagram of the Cu-S system, shown in Figure 2.4, contains the copper sulphide phases between cupric sulphide, CuS (covellite, CV) and cuprous sulphide, Cu_2S (chalcocite, CH). It is common to denote the copper sulphide as Cu_xS and then use the value of x to label the phases. At room temperature, there are three more stable phases between CuS and Cu_2S[34] which are ; djurleite (DJ), x = 1.96-1.94 ; the digenite (DG) $1.765 < x < 1.790$; and anilite (AN) x = 1.75 after Ref[35]. However, the compositional region of interest in solar cells extends from digenite to chalcocite. The defect structure of Cu_xS usually consists of a highly ordered sulphur sublattice with copper atoms in disordered site[36,37]. The digenite phase has a pseudocubic structure at room temperature whilst high digenite above $\sim 80^{o}C$ is cubic[35]. The djurleite phase is orthorhombic at room temperature, with a slow transformation at $93^{o}C$ to a tetragonal form[38]. The chalcocite is often considered to be orthorhombic,

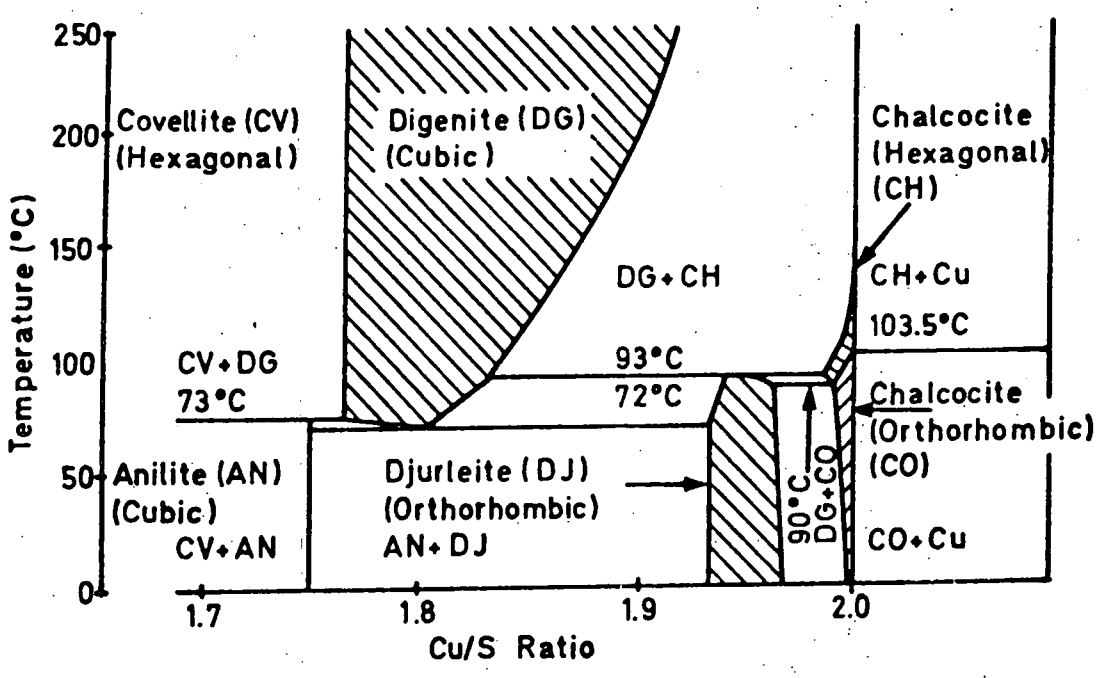


FIG. 2·4 THE PHASE DIAGRAM OF COPPER - SULPHUR SYSTEMS [34]

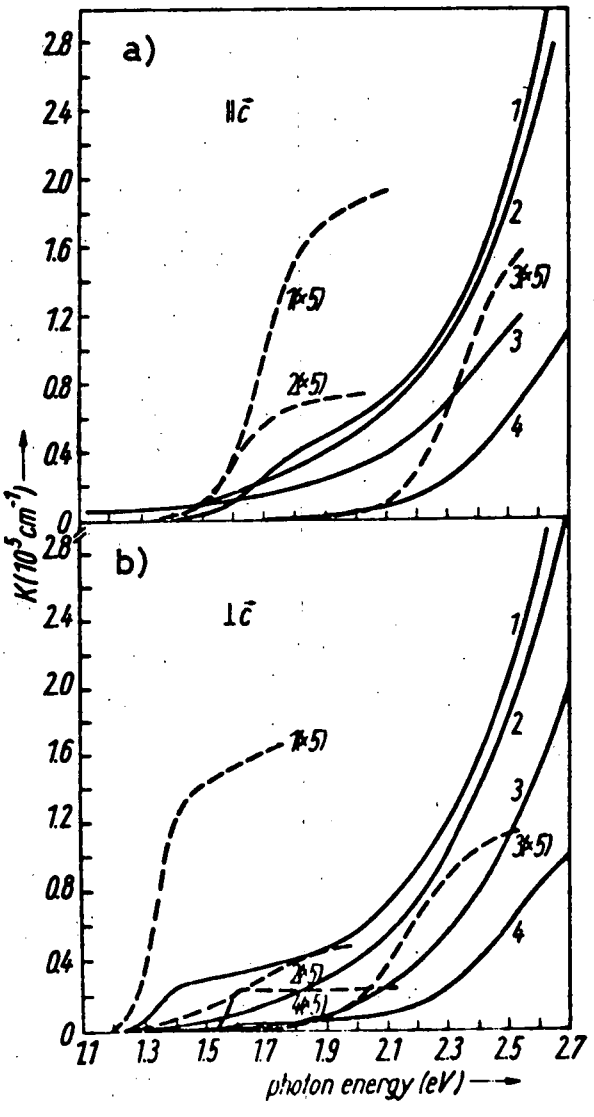


FIG. 2·5
CONTRIBUTIONS TO THE ABSORPTION COEFFICIENT (in cm^{-1}) FROM INTERBAND TRANSITIONS IN Cu_xS, THE LIGHT COMING a) PARALLEL, b) PERPENDICULAR TO C-AXIS. [46]

—— sum of the direct and indirect bands.
---- indirect band only.

1) CHALCOCITE
2) DJURLEITE
3) $Cu_{1.9}S$
4) DIGENITE

Evans[39] has shown that pure chalcocite is monoclinic. In detailed experiments, Cook et al[37] observed a mixture of chalcocite and djurleite in the compositional range $1.998<x<1.960$ which in the compositional range $1.960<x<1.800$ the structure appears to be hexagonal. They also demonstrated that the local atomic arrangement in djurleite is quite well matched to that in chalcocite. Furthermore, they found that the c-axis of low chalcocite and CdS match to within ½% but the a- and b-axes are mismatched by about 5%. Te Velde[40] gave a graphical illustration of the crystallographic relationship between copper sulphide and CdS. In fact the domain between djurleite and anilite is still under discussion and has been reviewed recently by Potter[34].

2.4.2 Optical Properties of Copper Sulphides

Stanley in 1975[43], Hill in 1978[42] and Savelli and Bougnot in 1979[43] have reviewed much of the reported data on the optical properties of various copper-sulphide phases. Although there is a large disparity between published results, a brief survey of data will be attempted.

Shiozawa et al[15] fitted their optical transmission measurments to an expression including a direct band to band transition at ∿1.8 eV and an indirect transition at 1.2 eV. Mulder[44,46,46] has measured the optical constants of single crystal copper sulphide of various compositions along different crystallographic directions. He concluded that the absorption of copper sulphide is highly anisotropic, and chalcocite (Cu_2S) is the only material with a large absorption coefficient in the photon energy region between 1.2 eV and 1.5 eV, and this occurs only when the direction of illumination is parallel to the c-axis (see Fig 2.5). Gustavino et al[47] demonstrated that the absorption coefficient in the infrared region decreases from 80% to 27% as the composition changes from chalcocite to djurleite. Mulder[46] suggested a band model with two types of transitions : indirect at around 1.2 eV and direct in the range of 2-2.5 eV. Loferski and Schewchun[48] considered that the transition in Cu_xS is more likely to be direct and

pointed out that the half-width of the cathodoluminescence peak in Cu_xS is rather narrow for an indirect semiconductor. Burton and Windawi [49] and Rothwarf and Windawi [50] supported this conclusion and claimed that their results were strongly indicative of direct gap behaviour. A comprehensive list of the values of the band gap of Cu_xS reported by various investigators is given in Table 2.2.

Mulder [46] has proposed a Moss-Burstein shift to explain the different band gaps of the copper sulphide phases. Thus he suggests that as the copper deficiency increases, the carrier concentration (hole) increases and with high copper deficiency the Fermi level enters the valence band giving rise to an effective direct energy band gap [46]. Kantariya et al [51] and more recently Rothwarf and Windawi [50] have also explained their observations by using the Moss-Burstein effect.

The two questions of the nature of the band gap as well as the magnitude of the gap still remain unsettled, largely because the absorption coefficient is not sufficiently large to suggest a direct band gap or sufficiently low to indicate an indirect gap. However, in spite of various conflicting reports the existence of one edge at 1.2 eV at 300 K is generally accepted in Cu_2S (chalcocite).

2.4.3 Electrical Properties of Copper Sulphides

Copper sulphide is a p-type semiconductor in which the conductivity is governed by copper vacancies regardless of its crystallographic structure. The electrical properties of copper sulphide, namely the electrical conductivity, Hall mobility, carrier concentration and thermo-electric power, have been measured by a number of workers. Published values of these parameters have been listed by Stanley [41] in 1975 and more recently by Savelli and Bougnot [43]. There is general agreement that dramatic changes in the electrical properties result following the departure from stoichiometry of chalcocite towards sulphur rich compositions. The most obvious features

TABLE 2.2 : A comprehensive survey of band gap values reported for copper sulphide (DIR ; direct, IND ; indirect).

Band Gap Value (eV)	T(K)	Nature of GAp	Structure	Measurement Techniques	References
1.21	300	IND	Evap.Film	Abs.Reflection	Eisenman (52)
1.21	300	IND	Cu doped CdS	Transmission	Bube (53)
1.21 1.26	300 80	IND IND		Transmission & Reflection	Marshal & Mitra (54)
1.21 1.83	300 300	IND DIR	Evap.Film of CdS and single cryst. CdS converted in wet tech	Trans & Reflec.	Schiozawa et al (15)
1.84 1.93	(300) 300	- -	Evap Film	Absorption Photo-Conductivity	Sorokin et al (55)
1.22 1.25	300 90	- -	Evap Film	Absorption and Refractive Index	Selle and Maege (56)
1.70 1.05	300 300	DIR IND	Evap Film	Absorption	Ramoin et al (57)
1.05 1.08	300 108	IND IND	Evap Thin Film	Trans & Reflec	Nakayama (58)
1.90	300	-	Bulk	Absorption	Abdullaev et al (59)
1.13(|| a-axis) 1.08(|| b-axis) 1.40(|| c-axis) 2.50	300 300 300 300	IND IND IND IND	CdS single Crystal converted by chemical conversion	Transmission & Reflection	Mulder (46)
1.28	77	DIR	Thin Layers Bulk	Cathodo-luminescence	Loferski et al (48)
1.46	120	DIR	Thin Layers	Trans & Abs.	Miloslawski (60)
1.21	300	-	Converted bulk	Trans & Abs	Gustavino et al (61)
1.15 2.29	300 300	IND DIR	Polycry. Thin Film	Trans,Reflec.	Arjona et al (62)

are an increase in the majority carrier density (copper vacancies) and the conductivity, and a decrease in the Seebeck coefficient.

Bougnot et al [63] demonstrated that the transition from semiconductor to semi-metal occurs at a composition of about $Cu_{1.95}S$. Reported values of carrier concentration range from $4x10^{15}$ cm^{-3} [58] to 10^{21} cm^{-3} [64]. Windawi [64] claimed that the value of 10^{21} cm^{-3} corresponds to a degenerate semiconductor with the Fermi level 0.2 eV inside the valence band. The variation of resistivity and thermoelectric power with the composition of Cu_xS have been studied by many workers [65,66,67]. In summary, the main conclusions are ; the resistivity and thermoelectric power of copper sulphides decrease almost linearly, from $9x10^{-2}$ Ω-cm to $2x10^{-3}$ Ω-cm and from 250 μV/°C to 60 μV/°C respectively in the composition range $2<x<1.95$. After then a slow linear reduction in ρ occurs from $2x10^{-3}$Ω-cm to $\sim 4x10^{-4}$ Ω-cm and in thermoelectric power from 60 μV/°C to 10 μV/°C as x ranges from 1.95 to 1.8. Abdullaev et al [59] and Bougnot et al [63] showed that the hole mobility is less dependent on stoichiometry, and reported values listed in Ref (41,43) which range from 1-30 cm^2/V-sec. More over the effective mass of holes in the copper sulphides increases slightly as the copper deficiency increases, going from about 1.5 m_o for chalcocite to about 2 m_o for digenite [63].

The diffusion length of minority carriers (electrons) (L_n) in the copper sulphides involved in practical CdS/Cu_xS cells, has been studied by several workers ; Gill and Bube [68] measured the short circuit photocurrent as a function of the distance of light spot from the junction, and estimated L_n to be between 0.1 μm and 0.4 μm. Mulder [69] determined L_n in a thin crystal sample of Cu_xS converted from single crystal CdS, and found a value of 300-350 Å for a chalcocite-djurleite mixture, and of less than 50 Å for djurleite. The electron beam induced current (EBIC) collected at the junction has also been measured in the SEM as a function of beam distance from the junction by many investigators. This provides a means of determining the minority carrier diffusion length on both sides of a Cu_xS/CdS heterojunction.

Böer et al [70] found values of electron diffusion such that $0.11\mu < L_n < 0.76\mu m$ in copper sulphide. Oakes et al [71] estimated that L_n lay between 0.11 μm to 0.57 μm. It has been reported consistently by Shea and Partain [72], Partain [73] and Partain et al [74] that L_n should be between 0.20 μm and 0.26 μm. Furthermore they concluded that heat treatment had no effect on L_n. In contrast Rothwarf [75] observed a change in L_n as the phase of copper sulphide changed . However studies of L_n following different heat treatments have as yet shown no conclusive variation.

There is a very little work on the electron affinity of copper sulphide. Schewchun et al [76] suggested the value of 4.05 eV by comparing cells based on Si-CdS and Si-Cu_xS. Pfiesterer et al [77] demonstrated that it is about 4.2 eV and Dunchemin et al [78] proposed a value of 4.4 eV.

The variation of the electrical properties with temperature has been analyzed by Gustavino et al [79] and found to be quite temperature dependent. At low temperatures (77 K) the thermal variation of the conductivity and the Hall mobility of Cu_2S are typical of a semiconductor. Further details can be found in Ref (40).

In an attempt to decrease the high value of carrier concentration in copper sulphides, Cd, Zn, and In have been used as dopants. Okomoto [66] demonstrated that indium plays the same role as Cu in Cu_xS. Gustavino et al [79] have studied the effects of Cd and Zn doping on the stable phases of Cu-S system and they concluded that Cd and Zn compensate copper vacancies and also displace copper atom to the surface. So that reduction in the free carrier density and the improvement in stiochiometry of copper sulphide is assumed to be beneficial for CdS/Cu_2S cells.

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CHAPTER 3

REVIEW OF RELEVANT THEORIES AND DISCUSSIONS

3.1 INTRODUCTION

This chapter reviews the theoretical background required for understanding various types of heterojunctions and their application as photovoltaic energy convertors.

The models proposed for CdS/Cu_2S and (CdZn)S/Cu_2S heterojunction cells are also surveyed. Although details are not given in great depth, an attempt is made to emphasize the physics by presenting a qualitative picture of the concepts involved and mathematical expressions are used only when necessary. In the main these are the expressions which will be used in the interpretation of results in the following chapters.

Heterojunctions are defined and classified in section 3.2 following the basic model of Anderson which forms the starting point for the more complex heterojunction theories. After this, a section on semiconductor-semiconductor interfaces and related phenomena emphasises the importance of the interfacial effects. The modification of the Anderson model to include the effects of interface states and dipoles, and the resulting carrier transport models, are presented in section 3.4. For completeness, the concept of a graded heterojunction is discussed in section 3.5 and then Schottky barriers are considered briefly in section 3.6. Concepts involved in the design of solar cells are discussed in section 3.7.

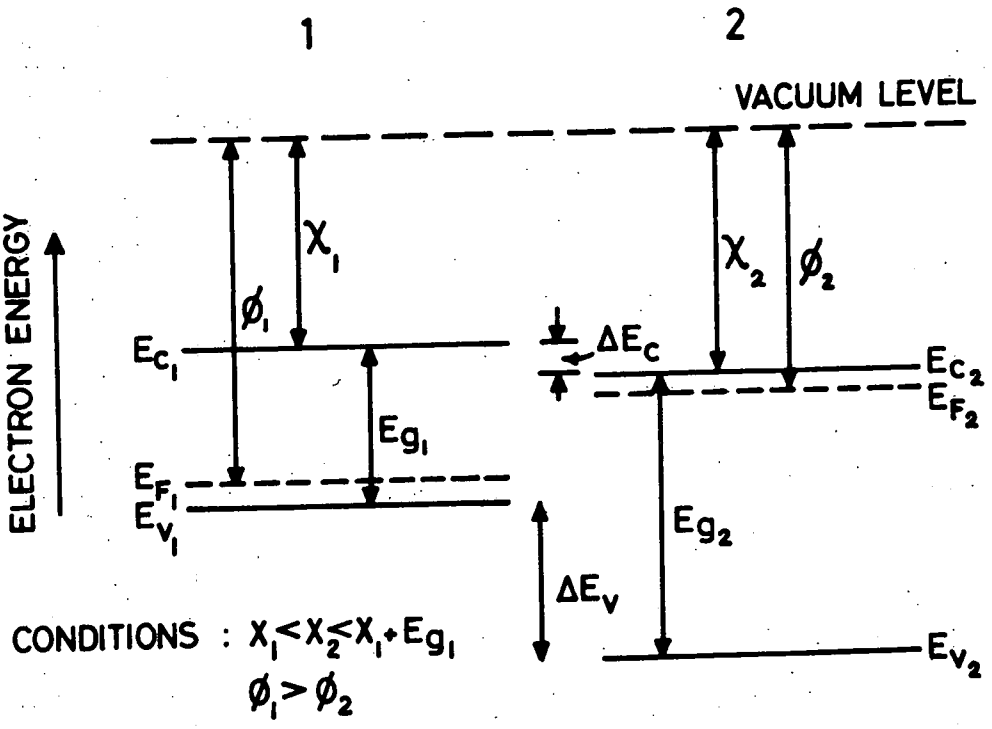
In the final section the various possible conduction mechanisms in CdS/Cu_2S and (CdZn)S/Cu_2S photovoltaic cells are summarised.

3.2 THE THEORY OF HETEROJUNCTIONS

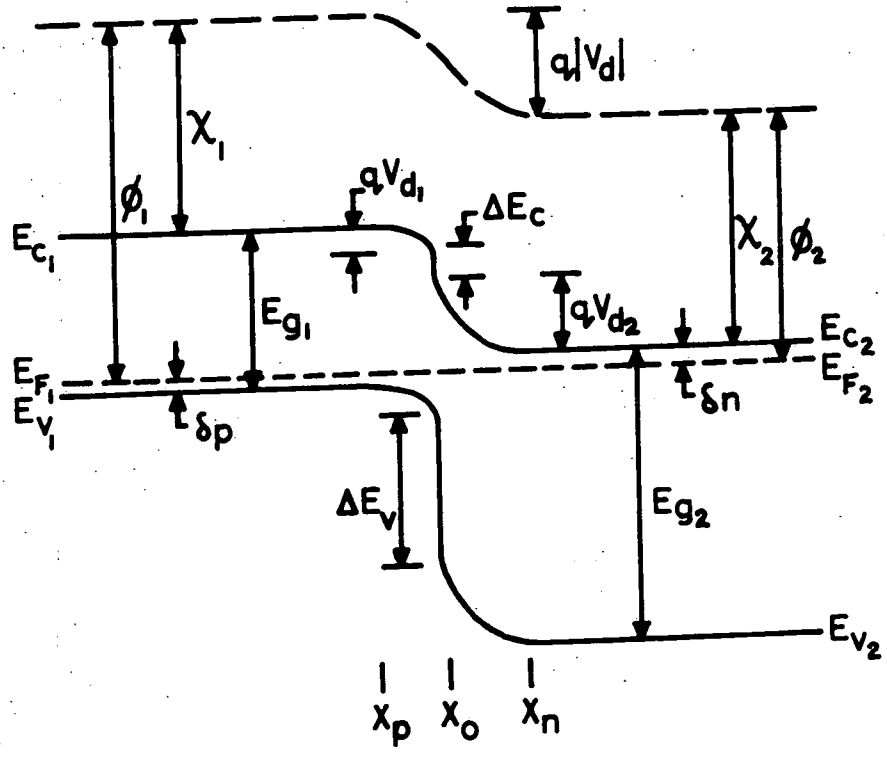
A heterojunction is defined as an electrical contact between two different semiconducting materials commonly taken to be monocrystalline. Heterojunctions may be classified in several ways. If there is non gradation in properties in passing from one material to another, the junction is described as "abrupt". If there is a gradual change in composition over macroscopic dimensions, the junction is "graded". Another classification involves the type of doping on either side of the junction, with similar dopings, i.e. n-n or p-p an isotype heterojunction is formed. With an-isotype junctions the components have different types of conductivity, so that n-p or p-n heterojunctions are formed (i.e. small band gap first).

The first isotype and anisotype heterojunctions were fabricated by Anderson[1] in 1960. He also presented[2] a fairly detailed model for the energy band profiles of the various heterojunctions. Although, most heterojunction phenomena cannot be explained by this simple model, and considerable discrepancy exists between theory and experiment, Anderson's model still forms the basis from which more complex and general models are usually developed.

The model for anisotype heterojunctions is a straight forward extention of the model developed for homojunctions. Anderson[1, 2] neglected the effect of dipoles and interface states. A typical energy band profile of two isolated pieces of p- and n-type semiconductor and theequilibrium energy band profile of an abrupt p-n junction formed by bringing them into intimate contact are shown in Fig. 3.1(a) and 3.1(b). The energy band profile in which a negative discontinuity step occurs in the conduction band edges at the interface is for the case in which $\chi_1 < \chi_2 < \chi_1 + Eg_1$ and $\phi_1 > \phi_2$. This is one of the many cases discussed by Milnes and Feucht[3]. Here the two semiconductors are assumed to have different energy gaps (Eg), different dielectric constants (ε), different work functions (ϕ) and



(a)



(b)

FIG. 3·1 (a) ENERGY BAND PROFILE FOR TWO ISOLATED SEMICONDUCTORS IN WHICH SPACE CHARGE NEUTRALITY IS ASSUMED TO EXIST IN EVERY REGION (b) SCHEMATIC ANDERSON HETEROJUNCTION MODEL AT EQUILIBRIUM (NO EXTERNAL VOLTAGE APPLIED)

different electron affinities (χ). The electron affinity (χ), and the work function (ϕ) are defined as the respective energies required to raise an electron from the conduction band edge (E_c), and from the Fermi level (E_F), to the vacuum level. E_v represents the top of the valence band. The subscripts 1 and 2 refer to the p-type (the narrow band gap) and n-type (the wide band gap) semiconducting materials respectively.

When two dissimilar semiconducting materials are brought into contact the flow of electrons from n-type to p-type and of holes from p-type to n-type, continues until equilibrium is established between p- and n-regions. When the Fermi levels on either side of the junction attain the same energy, electrons moving from the n-region have left behind an uncompensated positive space charge of ionized donors in the layer of width X_n, while holes moving from the p-region have left behind an uncompensated space change of ionized acceptor atoms in the layer of width X_p. As a result upward and downward bending of the respective band edges occurs. The total built-in voltage (V_d) due to the difference in work functions ($\phi_1 - \phi_2$) is equal to the sum of the built-in voltages on both sides ($V_d = V_{d1} + V_{d2}$) of the junction. It is interesting to note that in the absence of dipole layers the electrostatic potential difference (ψ) between two points is represented by the vertical displacement of the vacuum level between these two points. The discontinuity in the relative dielectric constants (ε_r) is easily dealt with by requiring that the electric displacement be continuous across the interface ($\varepsilon_1 F_1\big|_{x_o} = \varepsilon_2 F_2\big|_{x_o}$). Anderson's model predicts that band-edge discontinuities, ΔE_c and ΔE_v will occur depending on the electron affinities and band gaps of the two materials. The relation between these quantities is

$$\begin{aligned} \Delta E_c &= \chi_1 - \chi_2 \\ \Delta E_v &= \chi_2 - \chi_1 + E_{g2} - E_{g1} \end{aligned} \tag{3.1}$$

The depletion widths and capacitance can be obtained by solving Poisson's equation for either side of the interface. An exact solution of these equations requires numerical analysis which generally is not necessary. The most common approximations made are that, in the space charge regions, all the donors and acceptors are ionized and that for space charge computations, the free carrier density can be neglected. Hence the equations can be written :

$$-\frac{\partial^2 V}{\partial x^2} = \frac{\partial F}{\partial x} = \frac{q}{\varepsilon\varepsilon_o}\left[p(x) - n(x) + p_D(x) - n_A(x)\right]$$

$$\simeq \frac{q}{\varepsilon_2\varepsilon_o} N_D(x) \quad \text{for} \quad x_o < x < x_n \qquad (3.2)$$

$$\simeq \frac{q}{\varepsilon_1\varepsilon_o} N_A(x) \quad \text{for} \quad -x_p < x < x_o$$

Where the origin has been taken as the junction plane (X_o), and the variation of $N_D(x)$ and $N_A(x)$ with x is assumed to be a step function (abrupt junction approximation). From the charge neutrality condition ($N_A x_p = N_D x_n$) and eqn. (3.2), one can determine the width of each of the space charge regions, as a function of applied voltage $V=(V_1 + V_2)$. V_1 and V_2 are the portions of the applied voltage dropped on either side of the junction.

$$X_p = \left[\frac{2 N_{D2} \varepsilon_1 \varepsilon_2 (V_d - V) \varepsilon_o}{q N_{A1} (\varepsilon_2 N_{D2} + \varepsilon_1 N_{A1})} \right]^{\frac{1}{2}} \tag{3.3}$$

$$X_n = \left[\frac{2 N_{A1} \varepsilon_1 \varepsilon_2 (V_d - V) \varepsilon_o}{q N_{D2} (\varepsilon_1 N_{A1} + \varepsilon_2 N_{D2})} \right]^{\frac{1}{2}}$$

The total width, (W_d), of the transition region therefore is

$$W_d = X_n + X_p = \left[\frac{2 \varepsilon_1 \varepsilon_2 (N_{A1}^2 + N_{D2}^2) (V_d - V) \varepsilon_o}{q N_{D2} N_{A1} (\varepsilon_1 N_{A1} + \varepsilon_2 N_{A2})} \right]^{\frac{1}{2}} \tag{3.4}$$

The relative voltages supported in each semiconductor are

$$\frac{V_{d2} - V_2}{V_{d1} - V_1} = \frac{\varepsilon_1 N_{A1}}{\varepsilon_2 N_{D2}} \tag{3.5}$$

Since the junction has two conducting regions with a space charge barrier in between, it has a capacitance. The capacitance per unit area of such a completely depleted junction is given by

$$C = \left[\frac{q N_{D2} N_{A1} \varepsilon_1 \varepsilon_2 \varepsilon_o}{2(\varepsilon_2 N_{D2} + \varepsilon_1 N_{A1})(V_d - V)} \right]^{\frac{1}{2}} \tag{3.6}$$

Usually the bias voltage is dropped asymmetrically across the junction so that only one side is depleted.
Then the capacitance can be used to determine the corresponding donor or acceptor profile near the junction from the voltage dependence.

Anderson derived an expression for the current flow across a heterojunction in a manner similar to that used to derive the injection current in an ideal p-n homojunction. In the case shown (Fig. 3.1(b)) the transport of electrons will dominate and hole transport to the left is

neglected, with this assumption the current voltage relation for this diode is

$$J = q X N_{D2} \left(\frac{D_n}{\tau_n} \right)^{\frac{1}{2}} \exp\left(- \frac{q (\Delta E_c + V_d)}{kT} \right) \left[\exp\left(\frac{qV}{kT} \right) - 1 \right] \qquad (3.7)$$

Where V is the applied voltage, k, Boltzmann's constant, T, the absolute temperature, D_n and τ_n are the electron diffusion coefficient and lifetime in the p-region and X the transmission coefficient represents the function of the carriers with sufficient energy to cross the barrier.

Although the Anderson model is widely used to predict the configuration of the bands of heterojunctions, in many cases the experimental current-voltage relations are very different both in quality and magnitude from those predicted. Since an obvious modification to the Anderson model is to take into account the effects of interface states and dipoles, semiconductor-semiconductor interfaces will be discussed in the next section to provide a basis from which to discuss improved heterojunction theory.

3.3 SEMICONDUCTOR-SEMICONDUCTOR INTERFACES

Research on heterojunction, metal-semiconductor and metal-insulator-semiconductor structures shows that electrical transport is almost completely determined by the properties of very thin regions in the vicinity of the junction, including interface. The values of the electron affinities and the band gaps of the components give only a rough indication of the energy band structure of a heterojunction system. In the following sections an introduction to interface states, interface dipoles and oxide layers is given together with a brief discussion of interface related phenomena in heterojunctions.

3.3.1 Interface States

Interface states (or surface states) are defined as energy levels within the forbidden gap in the vicinity of the junction. These electrically active states would be expected to act either as charge traps, in which case a modified band profile would result, or as recombination centres affecting current transport and photoresponse, or both.

Interface states acting as charge traps, are considered to be donors if they are electrically neutral when filled with electrons and positive when empty. They are acceptor-like if they are neutral when empty, and negative when filled with electrons. In addition, interface states are classified into fast and slow states. The fast states exchange charge rapidly with the conduction or valence band and are assumed to lie very close to the interface between semiconductors. In contrast slow states require a longer time for charge exchange and exist up to several atomic distances from the interface. The electrical properties of interface states are characterised by their density, their position in the band gap and their capture cross section.

A breakdown of periodicity in a crystalline structure creates the most formidable defect in the region where two dissimilar materials come into intimate contact. Therefore a region with a drastic disruption of bulklike properties exists at the interface[4]. The parameters affecting interface formation and behaviour are microscopic, and specific features such as: lattice mismatch and mismatch defects (dislocations), localized charge and dipoles, band edge discontinuities and discontinuities in the electrostatic potential and its derivative, control the barrier.

Oldham and Milnes[5] were the first to stress the importance of mismatch dislocations on the ultimate behaviour of heterojunctions, and the electronic behaviour of dislocations has been discussed thoroughly in the book by Mataré[6]. In fact, a thin layer of material can be grown on a

substrate of a dissimilar crystollagraphic lattice to accommodate the strain elastically. But after a critical thickness, which depends inversely on misfit strain[4], it is energetically favourable to accommodate the strain plastically, generating dislocations at the interface.

The density of dislocations is directly related to lattice mismatch, and theoretical calculations show that a density of about 10^{13} states-cm^2 is expected for a lattice mismatch of 1%. The calculations of Oldham and Milnes[5] have been extended by Holt[7] to a discussion for the three dimensional case of mismatch dislocations in the diamond and sphalerite structures.

In principle, dangling bonds at the dislocation cores are to be expected. However Tansley[8] stated that dangling bonds in the densities predicted by Holt[7] would lead to an interface charge much larger than that measured experimentally, if all the mismatch dislocations were electronically active. Partial compensation must therefore take place, and only uncompensated interface charges account for the experimental observations. However, interface states are very effective, and even at low densities, when acting as recombination centres, they define the transport mechanism of carriers across the junction. Kressel[9] analysed the role of defects in optoelectronic heterojunction devices and Böer[10] has extended the calculation for CdS/Cu_2S and (CdZn)S/Cu_2S cells. A simple theoretical model[3] can be used to estimate the interface recombination velocity S_I for a given heterojunction from the lattice mismatch. The expression is

$$S_I = N_I^* v_{th} \sigma_c \qquad (3.8)$$

Where N^* is the density of interface states effective in the recombination process, σ_c is the mean capture cross section of the interface states and v_{th} the thermal velocity of the carriers.

Furthermore the interface and its vicinity are characterized by a very distinctive electrochemistry, especially in the initial stage of formation, this encompasses alloying, intermediate compound formation, localized diffusion of defects and impurities, and precipitation in the defective region. The effect of mismatch defects on the optoelectronic behaviour of heterojunctions is a field of research in which most of the questions are still open and most of the models proposed are purely speculative.

3.3.2 Interfacial Dipoles

Van Ruvyen[11] introduced the concept of the interfacial dipole in an attempt to understand heterojucntion interfaces. In this model it is assumed that the existence of a large number of surface states on the surface of the semiconductor is equivalent to a metallic layer which pins the Fermi Level. When these pseudo-metallic layers on each side of the junction are brought into intimate contact, dipoles of atomic dimensions are formed which are of the kind occurring at the interface between two bulk metals with different work functions.

The presence of a thin insulating layer also has a great influence on the structural properties of the interface as well as on the electronic behaviour of device. For example dipoles can form from the charge stored on the opposite side of a thin insulating layer at the interface, or from the spatial distribution of oppositely charged defects on either side of the interface in the bulk of the semiconductors[12].

Kroemer[13] analyzed bulk and surface properties separately assuming that electron affinities have two parts: the electron affinity of a hypothetically perfect crystal (bulk) and the electron affinity at the interface (corresponding to work done against surface dipoles). He criticized the approach in which the conduction and profile are determined by

the electron affinities of two semiconductors, and pointed out that for this situation to occur, the surface dipole layers of the two semiconductors must superimpose linearly without changing their strength, which is an unreasonable assumption because any dipole at the interface is different from such dipole at the free surface and consequently the band profile at the junction will be modified.

3.3.3 Oxide Layers

Native oxide layers are the most frequently occurring non-ideal features in semiconductor devices. The presence and thickness of the oxide, but most importantly, its structural and chemical characterists strongly affect the electronic behaviour of a device. There is a vast literature on the oxygen-semiconductor interaction particularly in silicon because of its technological importance. Thin oxide layers are extremely important in MIS solar cells and inexpensive, practical heterojunction devices (see ref (12) for further information).

3.4 MODIFICATION OF ANDERSON'S MODEL

The following sections show how Anderson's model has beeen extended to include interface states and dipoles in an attempt to resolve the discrepancy between the theory of heterojunctions and the experimental evidence.

Unfortunately, it is a very difficult problem to correlate the interface parameters in a heterojunction with its optoelectronic behaviour and the carrier transport. Because suitable experimental techniques are not available the electronic properties associated with interfacial defects cannot be measured directly, and are therefore estimated from indirect measurements using the proposed theoretical models which are purely speculative.

3.4.1 Junction Capacitance

A detailed theoretical analysis of junction capacitance with inclusion of interface states and dipoles has been given by Donelly and Milnes[14]. The results however have limited application because of the uncertainties associated with any model. Donelly and Miles showed, however, that in the limit where the interface charge is independent of applied voltage, the capacitance voltage relation takes the form

$$C^{-2} = \left[2 \left(\varepsilon_1 N_{A1} + \varepsilon_2 N_{D2}\right)/q\varepsilon_o\varepsilon_1\varepsilon_2 N_{A1} N_{D2} \right]\left(V_{di} - V \right) \qquad (3.9)$$

Here V_{di}, the diffusion voltage is modified by the charge stored at the interface, Q_{ss}, and the dipole voltage, ϕ_d, and is given by

$$V_{di} = V_d + \frac{Q_{ss}^2}{2q\left(\varepsilon_1 N_{A1} + \varepsilon_2 N_{D2}\right)} + \phi_d \qquad (3.10)$$

A plot of C^{-2} versus V then yields a straight line but the intercept on the $C^{-2} = 0$ axis is no longer a simple measure of the diffusion voltage (V_d). However the slope can be taken as a quantitative indication of the doping levels in the two components. The slope can be approximated by $2/q\ \varepsilon_2 N_{D2}$ for $\varepsilon_1 N_{A1} >> \varepsilon_2 N_{D2}$ and $2/q\ \varepsilon_1 N_{A1}$ for $\varepsilon_1 N_{A1} << \varepsilon_2 N_{D2}$.

The capacitance of CdS/Cu_2S heterojunctions with various space charge profiles has been investigated by Rothwarf[15].

3.4.2 Transport Mechanisms

The carrier transport mechanisms in heterojunctions which determine the current-voltage characteristics have been reviewed by several workers[8, 3, 12, 16, 17, 25]. When interface states and dipoles are included recombination through interface states seems to dominate the carrier transport mechanism in many heterojunctions.

The model proposed by Dolega[18] considers the junction as the interface between two surfaces, each having its own density distribution of surface states. The trapped charges, normally associated with surfaces, can recombine because of the overlap of the surface state distribution. Thus fast recombination occurs at the interface of those electrons and holes which reach the recombination centres by thermal emission over their respective barriers. Because of the fast recombination in the thin interfacial layer, no rectification is predicted unless the space charge region is wider than this layer. This model simply describes the heterojunction as two Schottky diodes back-to-back with the boundary concentrations of carriers dependent upon the applied voltage.

In order to reveal the general features of the forward current-voltage characteristic, Van Opdorp[19] has rewritten Dolega's expression in the form

$$J = B \exp\left(-\frac{q V_d}{kT}\right)\left[\exp\left(\frac{q V}{AkT}\right) - 1\right] \qquad (3.11)$$

Where A is the diode quality factor (it is conventional to use the symbol A for the quality factor for heterojunction and n for that of MS and MIS structures) with a value between 1 and 2, depending on the ratio of the density of imperfections in the two materials. B is a weakly temperature dependent coefficient. In this model the reverse current increases exponentially when the reverse voltage is increased. However, since this model implies thermal excitation over barriers, it cannot explain the temperature independent slopes of the Log J vs V curves observed for many heterojunctions. This temperature independence suggests that quantum mechanical tunnelling processes are more important.

A tunnelling mechanism to describe the current-voltage characteristics of an abrupt heterojunction was first introduced by Rediker et al[20].

This was based on electrons tunnelling through the conduction band spike to the p-type material. In the meantime Newman[21] found that an empirical expression for carrier transport in heterojunctions of the form

$$J = J_{so} \exp\left(\frac{T}{T_o}\right) \exp\left(\frac{V}{V_o}\right) \qquad (3.12)$$

Where J_{so}, T_o and V_o are constant, describes the current voltage characteristics of some heterojunctions very well. So that for many heterojunctions the mechanism seems to be the mixture of tunnelling and recombination. A model based on band to band tunnelling combined with recombination processes was first proposed by Riben and Feucht[22]. Fig3.2 summarizes various possible current paths for an anisotype heterojunction. The electron and hole processes e_1 and h_1 represent the diffusion model with the barriers modified by the band edge discontinuities. As already stated, such a process is not found to dominate experimentally although there is no reason to suppose that it cannot occur to a limited extend. The electron and hole paths e_2 and h_2 represent an emission and recombination situation in which the carriers are thermally excited into opposite ends of a ladder of interface states with a subsequent recombination; this mechanism is expected to show a temperature dependence. The third possibility illustrated by e_3, h_3 is a tunnelling process in which either the electrons tunnel from the conduction band of the wide band gap material into empty interface states located in the narrow band gap material (then recombine with holes) or holes tunnel from the narrow band gap (p-type) material into occupied states located in the n-type material (then recombine with electrons).

The spatial distribution of interface states has to be known within a resolution of 20-50 Å in order to establish whether the probability of tunnelling is involved in the various recombination pathways. But this

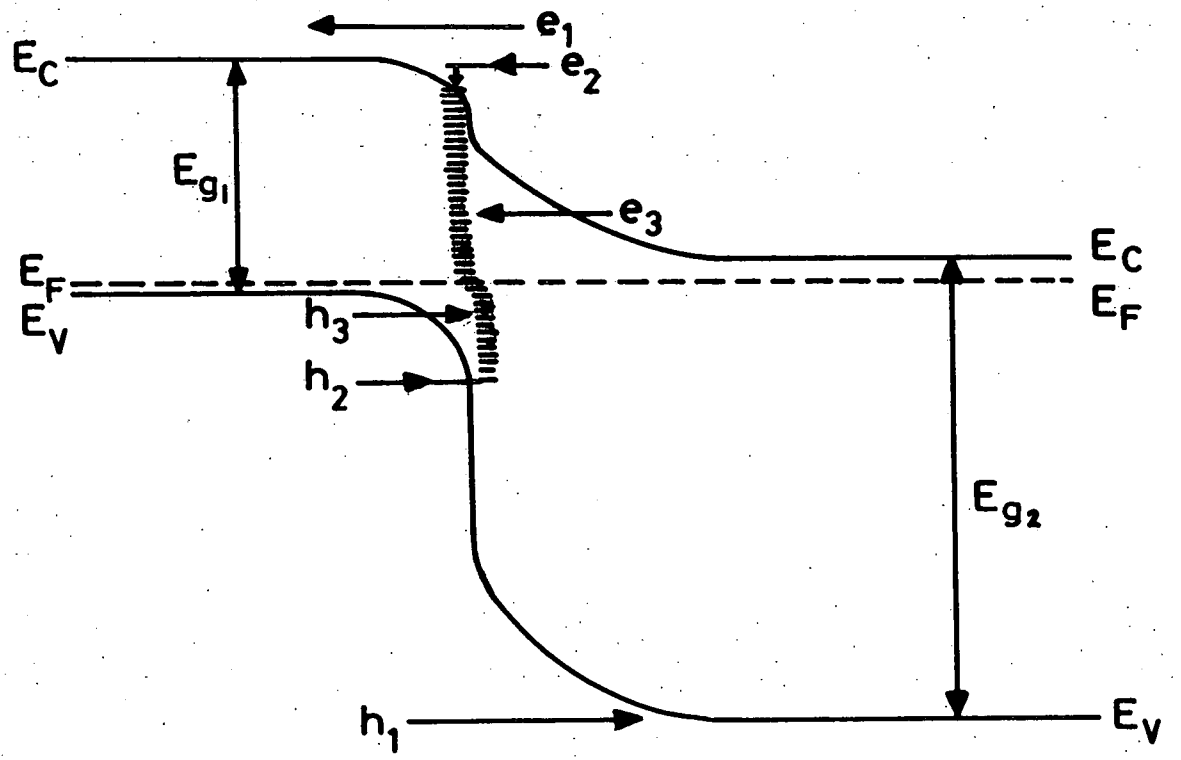


FIG. 3·2 POSSIBLE INTERFACE TRANSPORT MECHANISM IN ANISOTYPE HETROJUNCTIONS

is one of the features which has not been unambiguously revealed in any heterojunction structure.

Riben and Feucht[22] derived an equation using a triangular barrier and assuming that tunnelling originates from an energy level located at a certain distance above the bottom of the conduction band (E_b), and assumed the following relation to be appropriate in describing the current

$$J \propto N_i \exp \left[- 4(2m^*)^{\frac{1}{2}} E_b^{3/2} / 3 q \hbar F \right] \tag{3.13}$$

where N_i is the density of interface states, F the transition field with the remaining symbols have their usual meaning.

Riben and Feucht[23] and Donelly and Milnes[24] extended the theory to the multistep tunnelling-recombination model, and showed Eq. (3.13) would also be valid for tunnelling between spatially separated centres. Anderson[25] surveyed the existing transport models and proposed that if tunnelling originates at the bottom of the conduction band or the top of the valence band the dark forward current would be of the form

$$J = B \exp \left[- \alpha_T (V_d - V) \right] \tag{3.14}$$

where

$$\alpha_T = \frac{4}{3\hbar} \left(\frac{m_n^* \varepsilon_2}{N_{D2}} \right)^{\frac{1}{2}}$$

This expression for α_T assumes a single step process and a linear barrier. Agreement with experiment is generally poor. Using this model with an assumption of a linear barrier the reverse current has been written in the form [25]

$$J = C \exp \left[- A (V_d - V)^{-\frac{1}{2}} \right]$$

where

$$A = \frac{4}{3\hbar} \left(\frac{m_n^* \varepsilon_2}{N_{D2}} \right)^{\frac{1}{2}} E_{g2}^{3/2}$$

Here again, as with forward bias, a multi-step process must be postulated, and indeed the multi-step tunnelling recombination model[23] agrees more satisfactorily with experimental data. A simplified form of the appropriate equation is of the form

$$J_{tr} = C_f \exp(\beta T) \exp(\zeta V) \qquad (3.15)$$

where C_f is constant and the coefficient ζ and β are practically independent of the applied voltage and the temperature respectively. A current voltage relation of the equation (3.15) predicts that the slope of the $\ln J_{tr}$ versus V curves is almost temperature independent with the small remaining temperature dependence arising from the variation in the widths of the band gaps with the temperature.

Many heterojunctions exhibit a combination of two mechanisms: tunnelling-recombination, as discussed above, and thermal activation of carriers to higher energies where the barrier is thin enough for direct tunnelling to occur, or where direct access to the interface recombination centres obtains. Owen and Tansley[26] have analysed thermally assisted tunnelling in heterojucntion and concluded that the current voltage characteristics of abrupt anisotype $n\text{-}p^+$ semiconductor heterojunctions are similar to those n-type Schottky barrier diodes, provided the n-type regions are heavily doped ($N_D = 10^{17} - 10^{18}$ cm^{-3}). In this case charge carrier transport across the interface is governed by thermally assisted tunnelling through the depletion region of the n-type material.

3.5 GRADED HETEROJUNCTIONS

Semiconductor heterojunctions with gradual changes in composition over microscopic dimensions are called-graded heterojunctions. Very little theoretical work has been done to describe the energy band profile of such junctions and the possible current transport mechanisms. Because the abrupt heterojunction appears to be a good approximation for many heterojunctions which have been investigated, graded heterojunctions have not as yet been given much consideration. Recently however, Marfaing et al[27] and Buazzi et al[28] showed that devices with graded gap structures could considerably exceed their p-n heterojunction counterparts in solar efficiency. Hence the graded gap design has come to have greater interest in recent years. Reasons for grading the composition of a heterojunction are summarized by Fahrenbruch and Aranovich[12] as follows :

(1) to enhance the efficiency of conversion of photons over a distribution of wavelengths.

(2) to introduce an effective electric field in order to increase the diffusion length of minority carrier

(3) to spread the distribution of lattice mismatch states over a larger volume in order to decrease tunnelling between them, and thus reduce tunnelling recombination diode current.

(4) to eliminate the effects of conduction or valence band discontinuities.

3.6 SCHOTTKY BARRIERS

In order to avoid the complexity associated with heterojunctions complementary experimental work has been conducted on a Schottky barrier diodes. Thus in a preliminary study metal-semiconductor structures have been fabricated on CdS and then various aspects of these structures have been investigated to reveal key parameters relevant to the investigation of

heterojunctions based on CdS. It is necessary therefore to summarize Schottky barrier theory very briefly.

In Schottky barrier diodes the most important forward transport mechanisms are (considering n-type semiconductors only) :(I) thermionic emission of electrons from the semiconductor over the top of the barrier into the metal. (II) recombination in the depletion region. (III) quantum mechanical tunnelling through the barrier. (IV) minority carrier (hole) injection. The transport of carriers might be limited by diffusion or thermionic emission according to the width of space charge region[29].

If the space charge region is thinner than the diffusion length, the thermionic emission limited forward current will be of the form[30]

$$J = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{3.16}$$

The Schottky barrier height ϕ_B is approximately equal to the difference between the metal work function and the electron affinity (χ_s) of the semiconductor, while A^* is the modified Richardson constant, corresponding to the effect mass (m^*).

$$A^* = 4\pi q m^* k^2/h^3 = 120 \frac{m^*}{m_o} \text{ amp/cm}^2 \text{ K}^2 \tag{3.17}$$

when the space charge region is thicker than the diffusion length the dark forward current is limited by diffusion and the J-V relationship becomes

$$J = q N_c \mu_e F_{max} \exp\left(\frac{-q\phi_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{3.18}$$

Here F_{max} is the maximum electric field at the junction, μ_e the electron mobility and N_c the effective density of states in the conduction band

$$N_c = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2} \tag{3.19}$$

In many barriers, of course, these mechanisms are combined when the space charge region is comparable in thickness to diffusion length[30], then

$$J = \frac{q N_c \nu_R}{1 + \nu_R/\nu_D} \exp\left(\frac{-q\phi_B}{kT}\right) \exp\left[\left(\frac{qV}{kT}\right) - 1\right] \qquad (3.20)$$

where $\nu_R = A^* T^2/qN_c$ is the effective recombination velocity and ν_D the effective diffusion velocity.

In fact, the experimental forward characteristic is usually written

$$J = J_o \left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \qquad (3.21)$$

The Schottky diode quality factor, n, shows a deviation from unity even in the ideal case because of the small lowering of the actual barrier height by the image force effect which is field dependent. Non-ideal diode mechanisms such as recombination in the depletion region and tunnelling will not be discussed. A detailed treatment can be found in the book by Rhoderick[31].

The utilization of metal-semiconductor devices for solar cell applications is very attractive because of the simplicity of the structure and its inexpensive technology, but the low value of V_{oc} is a difficult problem to overcome.

3.7 HETEROJUNCTIONS AS PHOTOVOLTAIC ENERGY CONVERTORS

A precise description of the operation of heterojunctions as photovoltaic energy convertors is quite complex. The normal procedure is to consider the ideal solar cell case in order to establish the relations between the observable electrical parameters of a heterojunction and the conversion efficiency of a heterojunction solar cell. The usual approach

to the problem is to treat it by making a linear superposition of the light generated current and the dark diode current assuming thermal equilibrium. In the later part of this section, the light generated current will be calculated using the simplified form of the diffusion equations. Then an equation will be derived to describe how the current-voltage characteristics of a heterojunction solar cell can be related to its equivalent circuit. Finally the definition of the efficiency and the solar spectrum will be given.

3.7.1 Light Generated Current (J_{LO})

For simplicity, it is assumed that all useful generation in the CdS/Cu_2S cell occurs in the p-type (narrow band gap) material, of thickness x and optical absorbtion coefficient $\alpha(\lambda)$, with radiation of intensity I_o and energy $h\nu$ incident normally on its free face. The number of photons absorbed per unit time per unit volume is then $I_o\alpha(\lambda)/h\nu$ The relation between the number of electron-hole pairs produced and the number of photons absorbed is defined as the quantum efficiency, Q.

In the steady state, the bulk generation and recombination rates for electrons and holes are equal. Thermo-dynamic equilibrium holds within the bands and the carrier relaxation time ($\tau_r \approx \mu m^*/q \approx 10^{-13}$s) is much smaller than the effective minority carrier life time τ_n. The recombination rate can be represented by a linear function such as $\Delta n/\tau_n$ in the p-type and $\Delta p/\tau_p$ in the n-type material. For an ideal heterojunction the total current flowing across the junction is

$$J = J_o\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \qquad (3.22)$$

Where the pre-exponential reverse saturation current is (Ref.30).

$$J_o = \frac{q D_p p_n}{L_p} + \frac{q D_n n_p}{L_n} \qquad (3.23)$$

Here, $L_n = (D_n \tau_n)^{\frac{1}{2}}$, $D_n = \mu_n kT/q$ are the diffusion length and the diffusion constant for electrons in p-region, and $L_p = (D_p \tau_p)^{\frac{1}{2}}$, $D_p = \mu_p kT/q$ are the corresponding quantities for holes in n-region. n_p, p_n represent the electron and hole concentration in the p- and the n-regions respectively.

The carrier densities increase under illumination fron n_p to $n_p + \Delta n_p$ and from p_n to $p_n + \Delta p_n$ due to the absorbtion of photons. Hence the saturation current density under illumination becomes:

$$J_o' = \frac{q L_p}{\tau_p} (p_n + \Delta p_n) + \frac{q L_n}{\tau_n} (n_p + \Delta n_p) \qquad (3.24)$$

or

$$J_o' = J_o + \left(\frac{q L_p \Delta p_n}{\tau_p} + \frac{q L_n \Delta n_p}{\tau_n} \right)$$

so the photogenerated current is given by

$$J_{Lo} = q \left(\Delta p_n \frac{L_p}{\tau_p} + \Delta n_p \frac{L_n}{\tau_n} \right) \qquad (3.25)$$

If equation (3.25) is rearranged taking into account that

$$\Delta n_p = \frac{I_o \alpha(\lambda) Q \tau_n}{h\nu} \quad \text{and} \quad \Delta p_n = \frac{I_o \alpha(\lambda) Q \tau_p}{h\nu}$$

it becomes

$$J_{Lo} = \frac{I_o \alpha(\lambda) Q}{h\nu} q (L_n + L_p) \qquad (3.26)$$

The magnitude of the light generated current, and hence the performance of the solar cell is determined by a multitude of factors, these include: (1) the intensity and spectral distribution of the incident light, (2)the reflection from the cell layers, (3) the specific absorbtion of the active layers, (4) the bulk and surface recombination processes, (5) the mobility of the carriers, (7) gross defects such as grain boundaries and cracks in the active materials. In fact J_L (essentially the short circuit current $\sim J_{sc}$) is important in determining the power output of the cell, and the relation between the light generated current J_{Lo} and J_{sc} is controlled by the interface collection factor, since $J_{Lo} = J_{sc} + J_{Lr}$ where J_{Lr} is the return current path to the p-type material via the interface states. At the junction we can write $J_{Lr} = q\, S_I\, n_I$ where n_I is density of electrons at the junction, S_I the effective interface recombination velocity and $J_{sc} = q\, n_I\, \mu_2\, F_2$ where F_2 is the field at the junction (n-region) in the light and μ_2 is the electron mobility in n-type material. Thus the relationship between J_{Lo} and J_{sc} becomes

$$J_{sc} = J_{Lo} \frac{\mu_2 F_2}{S_I + \mu_2 F_2} \qquad (3,27)$$

As may be seen in equation 3.27 the field F_2 ($F_2 = \frac{2 V_D}{W_d}$) at the junction and the interface recombination velocity are the key parameters in determining the fraction of light generated current which forms the measured short circuit current.

3.7.2 Equivalent Circuit and Diode Equation

In the previous section the discussion has been concentrated on unilluminated p-n junctions, neglecting a series, R_s and parallel shunt resistance, R_{sh}. In fact, considerable series resistance may arise from

the bulk n- and p-layer and from contacts. Losses occurs from the junction leakage and change the current paths via parallel or shunt resistance across the diode. The solar cell is usually presented as a light dependent current generator in parallel with a diode and the additional series and parallel resistance, so that the resulting equivalent circuit is as shown in Fig. 3.3. where R_L represents a load resistance. When a junction is illuminated, the light generated current is usually assumed to be added linearly to the dark diode current, so that the characteristic shifts downwards, and the intersections of the curve with the current and voltage axes are called the short circuit current, J_{sc} and open circuit voltage, V_{oc} respectively. The effects of R_s and R_{sh} on the light current-voltage characteristics of the cell are displayed in Fig3.3(a). Thus taking these effects into account it is common practice to write the current voltage relationship under illumination as

$$J = \sum_i J_{oi} \left[\exp\left(\frac{q\,(V-JR_s)}{A_i\,kT} \right) - 1 \right] + \frac{V - JR_s}{R_{sh}} - J_{sc} \qquad (3.28)$$

Here J is the current density, J_{oi} and A_i are the current and diode factors for ith mechanism, V is the voltage across the device, and other parameters have their usual meanings.

3.7.3 Efficiency of Solar Cells and Fill Factor

Fig. 3.4 shows typical dark and light J-V. characteristics for a solar cell defining the open circuit voltage (V_{oc}) short circuit current (J_{sc}). The maximum of the current voltage product on the light J-V curve gives the maximum power point, J_m, V_m. Thus the maximum power output of the cell can be represented by the shaded rectangle, and defined as $P_{max} = J_m V_m$, and the efficiency, η, of a solar cell is

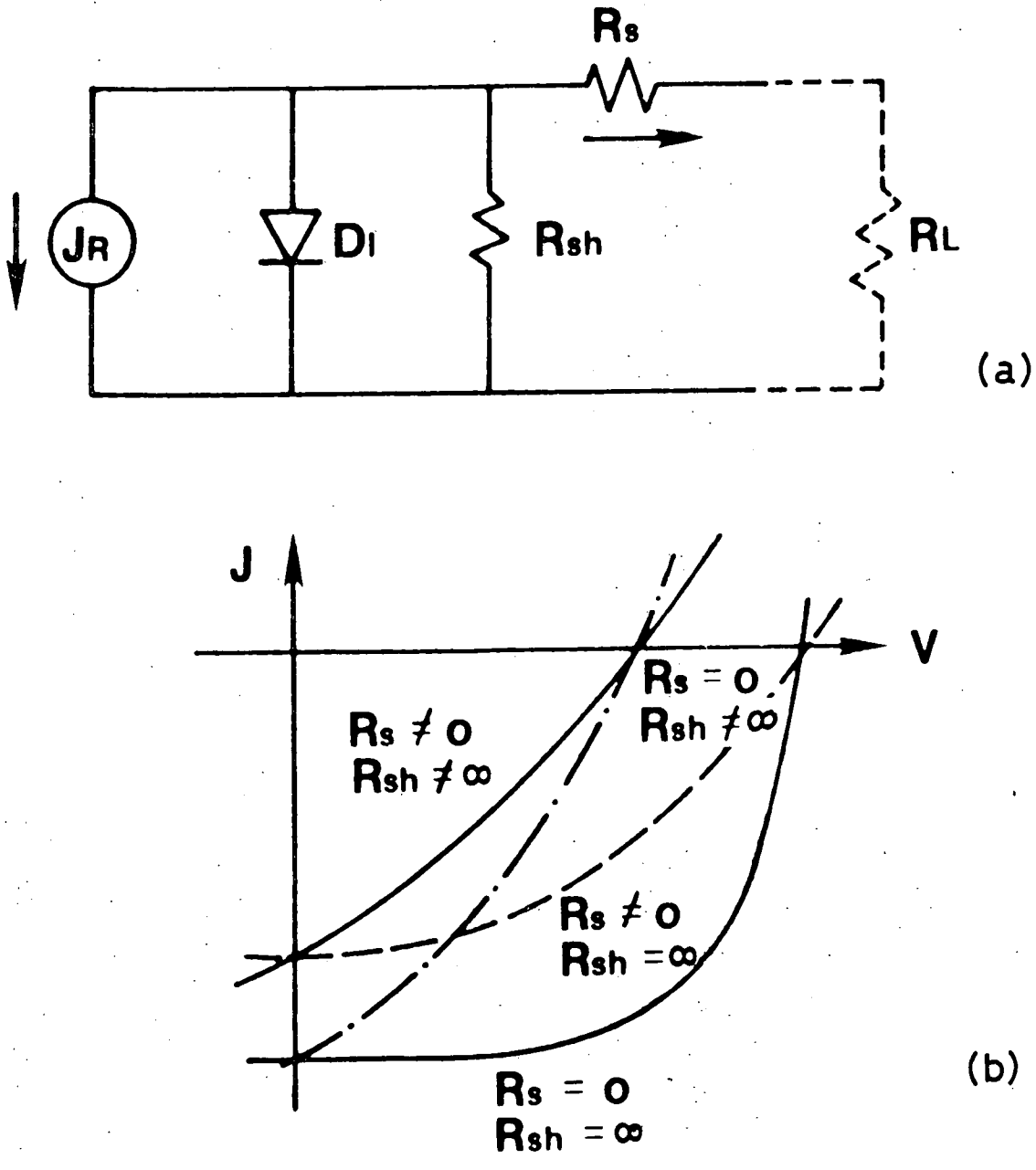


FIG. 3·3 (a) SIMPLIFIED EQUIVALENT CIRCUIT FOR SOLAR CELLS.

(b) J - V CHARACTERISTICS, UNDER ILLUMINATION, INDICATING EFFECTS OF CHANGING SERIES AND SHUNT RESISTANCE.

then the ratio between the electric power which can be extracted at the maximum power point and the input power density (usually expressed in mW cm^{-2}), $\eta = {}^{P_{max}}/_{P_{in}}$. The maximum power output can be written in terms of J_{sc} and V_{oc} as $p_{max} = J_{sc}V_{oc}x$ (Fill Factor), here the fill factor is given $FF = ({}^{J_m V_m}/_{J_s V_{oc}})$. In practice J_{sc}, V_{oc} and FF are not totally independent of one another. For an ideal situation with neglecting series resistance and shunt conductance and one dominant mechanism equation (3.28) becomes

$$J = J_o \left[\exp\left(\frac{qV}{AkT} \right) - 1 \right] - J_{sc} \tag{3.29}$$

so that V_{oc}

$$V_{oc} = \frac{AkT}{q} \ln \left(1 + \frac{J_{sc}}{J_o} \right) \tag{3.30}$$

The condition for maximum power output is

$$\frac{d}{dV} (J\ V) \Big|_{V=V_m} = 0 \tag{3.31}$$

$$\text{i.e.} \quad \frac{d}{dV} \left\{ \left[J_o\ V \left(\exp\left(\frac{qV}{AkT} \right) - 1 \right) \right] - J_{sc}\ V \right\} \Bigg|_{V = V_m} = 0 \tag{3.32}$$

since $J_{sc}/J_o >> 1$ the solution of Eq. (3.32) can be written as

$$\left(1 + \frac{q\ V_m}{AkT} \right) \exp\left(\frac{q\ V_m}{AkT} \right) = \frac{J_{sc}}{J_o} \tag{3.33}$$

Similarly the current density J_m for the maximum power can be found by differentiating the maximum output condition for current.

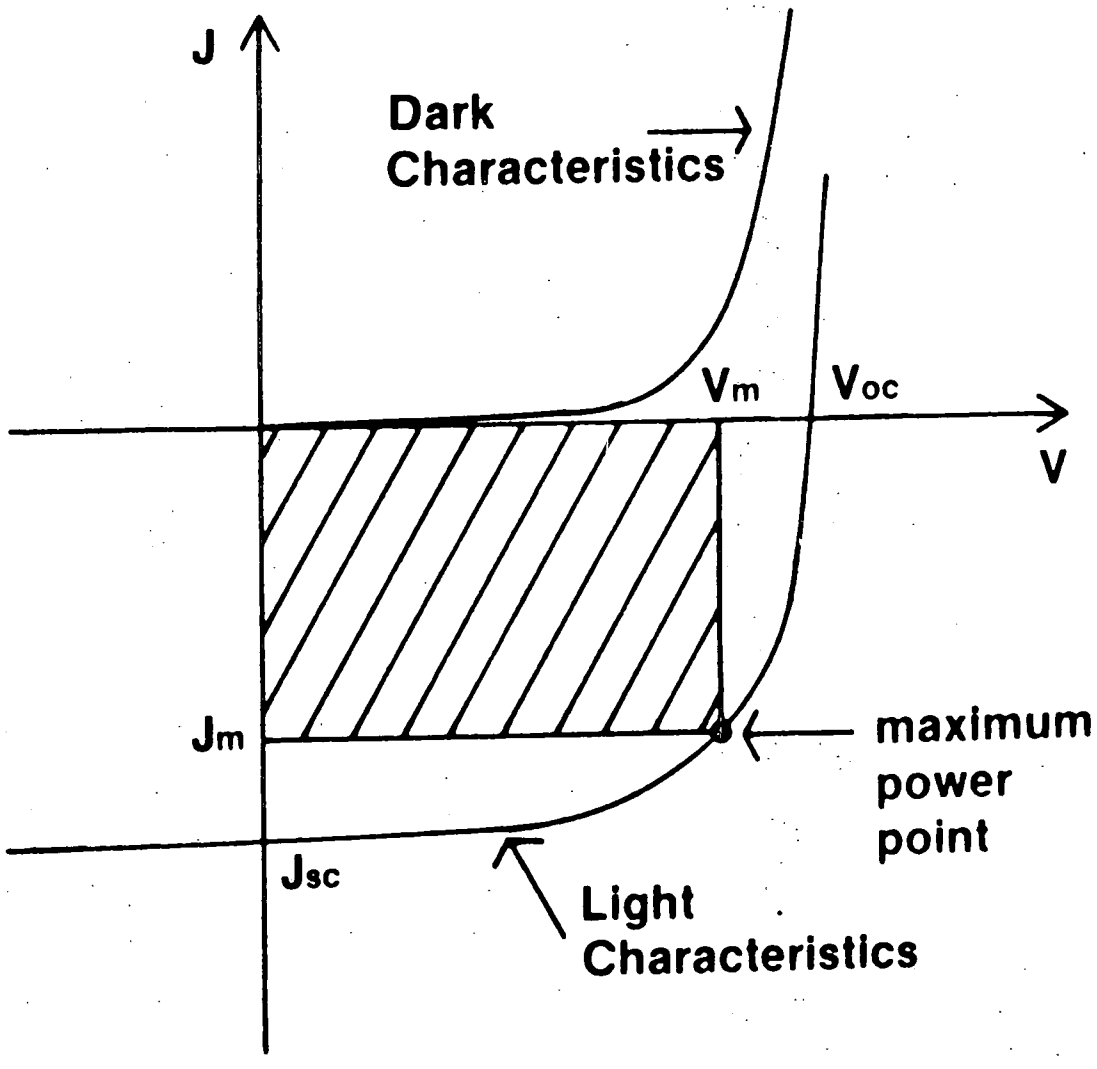


FIG. 3·4 LIGHT AND THE DARK J - V CURVES FOR SOLAR CELLS

The current at the maximum power point is,

$$J_m = J_{sc} - J_o \left[\exp\left(\frac{q V_m}{AkT}\right) - 1 \right] \tag{3.34}$$

So that the fill factor can be written

$$FF = \frac{J_m V_m}{J_{sc} V_{oc}} = \frac{V_m}{V_{oc}} \left\{ 1 - \frac{J_o}{J_{sc}} \left[\exp\left(\frac{q V_m}{AkT}\right) - 1 \right] \right\} \tag{3.35}$$

but

$$J_{sc} = J_o \left[\exp\left(\frac{q V_{oc}}{AkT}\right) - 1 \right] \tag{3.36}$$

Thus Eq. 3.35 becomes

$$FF = \frac{V_m}{V_{oc}} \left\{ 1 - \frac{(\exp(q V_m/AkT) - 1)}{(\exp(q V_{oc}/AkT - 1)} \right\} \tag{3.37}$$

Once J_{sc} is known all parameters of the ideal solar cell can readily be determined from the J-V characteristics. As is clear from the treatment above, the diode factor A and the current factor, J_o are the most effective indicators linking the solar efficiency and the electrical properties of the junction.

3.7.4 Solar Radiation

The spectrum of sunlight extends from the ultraviolet through the visible to the far infrared as shown in Fig 3.5(Ref (32)). Solar light just outside the earth's atmosphere is described as having an intensity of air mass 0 (AM0) corresponding to 138 mW/cm^2. The air mass 1 (AM1) spectrum represents the sunlight at the earth's surface for optimum weather conditions with the sun at the zenith, leading to radiation with an intensity of about 100 mW/cm^2. The air mass 2 (AM2) spectrum in Fig 3.5 represents the sunlight

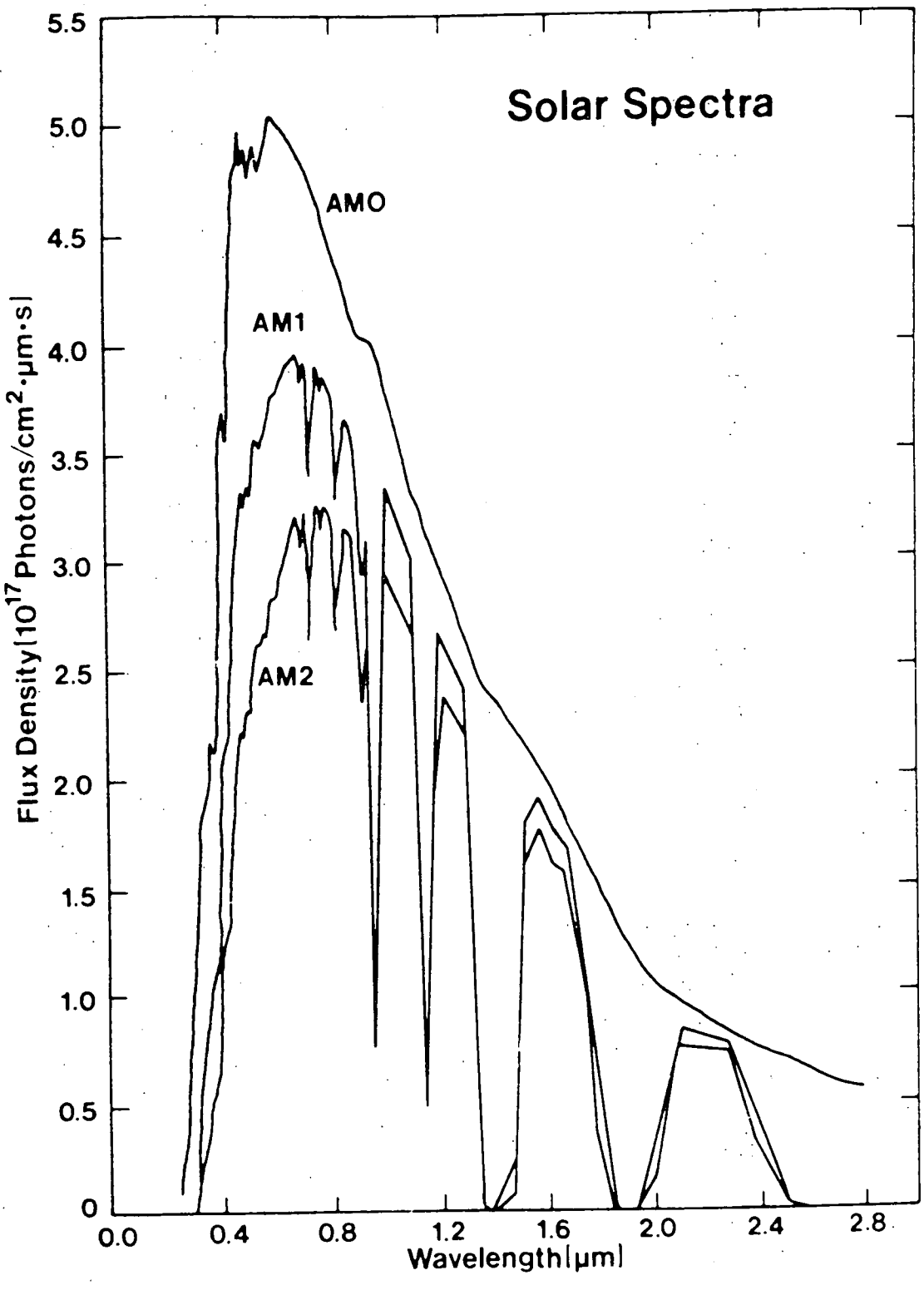


FIG. 3·5 THE SOLAR SPECTRUM OUTSIDE THE ATMOSPHERE (AMO), AT SEA LEVEL (AM1) AND FOR AVERAGE ATMOSPHERE CONDITIONS (AM2)

received at the earth's surface when the sun is at an angle of 60°, leading a total incident power of 72-75 mW/cm^2. The major differences between sunlight in space and at the earth's surface are that ultraviolet light is filtered out by ozone in the upper layer of the atmosphere and infrared removed from spectrum by water vapour and CO_2.

3.8 MECHANISMS IN CdS/Cu_2S AND $(CdZn)S/Cu_2S$ PHOTOVOLTAIC CELLS

The CdS/Cu_2S photovoltaic cell has been under continuous study since its discovery three decades ago[33], and following the report by Palz et al[34], the $Zn_xCd_{1-x}S$ alloy is also being investigated intensively as a better collector material for the Cu_2S absorber since this combination offers the potential of higher open circuit voltages. Some of the many models put forward to explain the conduction mechanism in the CdS/Cu_2S junction are summarised below.

The concept of the CdS/Cu_2S heterojunction was first proposed by Cusano[35] and supported by Keating[36]. Before that Woods and Champion[37] and Grimmeis and Meming[38] had suggested that the CdS/Cu_2S cell operated as a p-n homojunction i.e. there p-type layer of CdS was formed by heavy copper diffusion into an n-type substrate. Williams and Bube[39] also suggested that the phenomenon was associated with some kind of metal semiconductor junction. Then evidence from the Philips Labs.[40] and from the Clevite Corp.[41] confirmed that the device was indeed a p-n hetero-junction of CdS/Cu_2S. Since then the various models proposed to describe the conduction mechanism in CdS/Cu_2S structures have been summarised by several workers : Crossley et al. (1968)[42], Van Aeorschodt et al (1971)[41], Stanley et al (1975)[44], R. Hill (1978)[17], Savelli et al (1979)[45].

At the conclusion of the Clevite research programme for NASA on the mechanism of the photovoltaic effect in CdS/Cu_2S devices the level of under-standing was summarised by the so-called Clevite model of Shiozawa et al[46]. Many of the basic ideas incorporated into this model remain valid. In the Clevite model the cells were essentially considered to be p-i-n junctions,

with a nearly degenerate p-type layer of cuprous sulphide with a thickness of about 0.3 μm, an approximately intrinsic layer of cadmium sulphide (∿1 μm) compensated by copper produced during a sensitising bake at 200°C and an n-type layer of cadmium sulphide Fig.3.6. Shiozawa et al[46] proposed that the major photocurrent was generated in the cuprous sulphide layer and that the cell was basically an anisotype heterojunction. In order to explain most of the experimental observations, the Clevite model relied heavily on the idea of an intrinsic i-layer in the cadmium sulphide because the measurement of the rate of copper diffusion in CdS suggested that the CdS close to the junction would be quite strongly compensated by copper acceptor centres. Thus this layer would be photoconductive and introduce an illumination dependent series resistance and a junction barrier height which changed under illumination. In addition, the i-layer would affect the spectral response and response time of the cell. A similar model was proposed by Mytton[47]. Gill and Bube[48] and Van Aershodt et al[43] criticised the Clevite model in connection with the non-observation of the series resistance of the i-layer in high forward current in the dark. Moreover, the increase in the short circuit currents at very low levels of illumination and the long persistence of photocurrent enhancement effects by secondary light cast doubt on the Clevite model. As a result Van Aershodt et al.[43] suggested a model in which the barrier height and the occupancy of interface states changed under illumination.

In an early model proposed by the Stanford group (Bube and his co-workers form the Stanford group)[48, 49, 50], it was considered that the heterojunction had a conduction band spike and that tunnelling through this spike and recombination via interface states played the major role in determining the mode of current transport. It was assumed that after heat treatment, the tunnelling probability was controlled by the occupancy of deep levels in the CdS depletion region at 0.3 eV and 1.1 eV above the

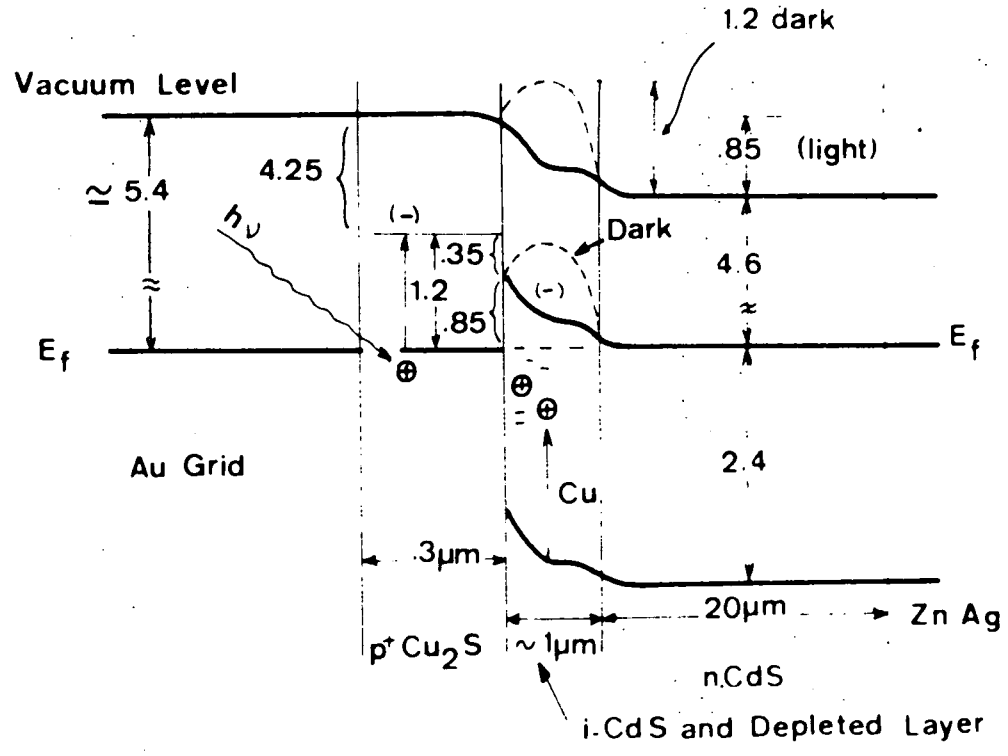
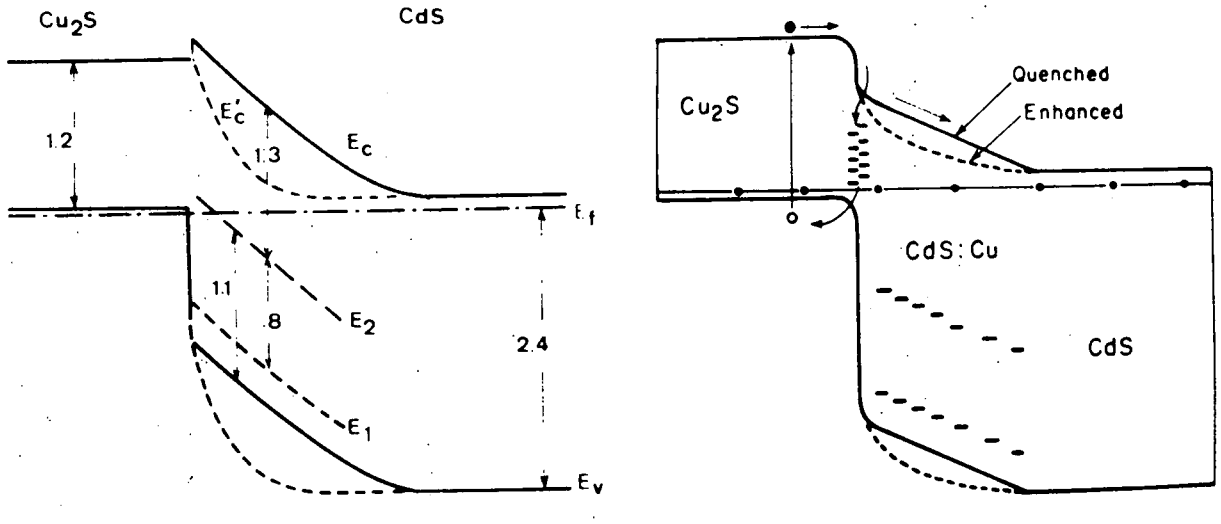


FIG. 3·6 CLEVITE MODEL [46] (Energy in eV)



(a) the early model (b) the recent model

FIG. 3·7 STANFORD MODEL [48,52] (Energy in eV)

valence band. In the dark, acceptor impurities widen the depletion layer reducing the dark current. Illumination decreases the depletion width and restores the forward current, Fig 5.7(a). Later Fahrenbruch and Bube[51] emphasised the dominance of tunnelling-recombination current through interface states and deep levels, which were caused by lattice mismatch and the diffusion of copper into CdS, respectively. However a more recent major modification is the assumption of a negative conduction band discontinuity instead of a spike. The recent model described by Bube[52] is shown in Fig. 5.7(b). Haines and Bube[53] have investigated the parameters controlling the photovoltaic properties of CdS/Cu_2S heterojunctions and concluded that the behaviour of J_{sc} and V_{oc} is describable in terms of a deep donor like level (with an ionization energy of about 0.45 eV) in the CdS region adjacent to the metallurgical interface. The effects of these centres were summarized as: (I) Deep levels can greatly increase tunnelling currents by producing the large electric field near the interface and by shortening the required tunnelling distance. (II) They may also act as interface recombination centres. (III) They change the interface collection efficiency.

Massicot[54] proposed a model with an interlayer material with a band gap of 1.8 eV (probably $Cu_{1.95}S$, djurleite) which can be created and dissipated at the interface by a thermal and photochemical processes respectively. This model was also used to discuss the high voltage cells reported by Chamberlin et al[55].

Te Velde[56, 57] has investigated the CdS/Cu_2S structures and discussed the effects expected if the conduction band discontinuity changed from a notch to a spike. He assumed that during the sensitizing heat treatment while copper diffuses into CdS, oxygen penetrates to the junction interface where it forms electron traps. As this takes place the barrier between CdS/Cu_xS increases. For the case of a notch in the conduction band,

te Velde found that the electron current injected into the CdS is small compared to the recombination current at the junction. Thus the relationship between the interface recombination velocity and the velocity of electrons at the top of the barrier defines the amount of photogenerated current crossing the junction into CdS. He also concluded that the open circuit voltage should increase as the notch in the conduction band decreased Fig 3.8. When a spike in the conduction band appears at the junction, te Velde showed that the photocurrent collection efficiency should decrease as the spike height increases, whilst the open circuit voltage should remain independent of spike height. The optimum case should be reached when the conduction bands are lined up (Fig.3.8). Deb et al[58] have analysed te Velde model[56] with interface states caused by oxygen trapping at the interface, to explain the improvement of the performance of the cell with different heat treatments.

Martinuzzi et al.[59, 60] have adopted the model of multi-step tunnelling through interface states proposed by Riben and Feucht[22], to explain the transport mechanisms in CdS/Cu_2S cells in single crystal and thin film forms. Since the tunnelling mechanism seemed to be reduced when CdS single crystals were used they concluded that localized levels related to crystallographic defects, assisted in the multi-tunnelling. With the CdS/Cu_2S single crystal photovoltaic cell (Fig 3.9), Martinuzzi et al[60] have proposed that the diffusion potential is 0.82 eV and that the junction has a notch in the conduction bands with a depth 0.14 eV, resulting in a valence band discontinuity of 1.34 eV. They found that the Fermi level was 0.12 eV below the conduction band in the bulk CdS and 0.15 eV below the conduction band in the depletion region, suggesting that only slight compensation occurred in these single crystal cells. They also showed that at low forward bias and room temperature, thermal activation was required, with the activation energy of 0.65 eV, in order fully to explain the forward current mechanism.

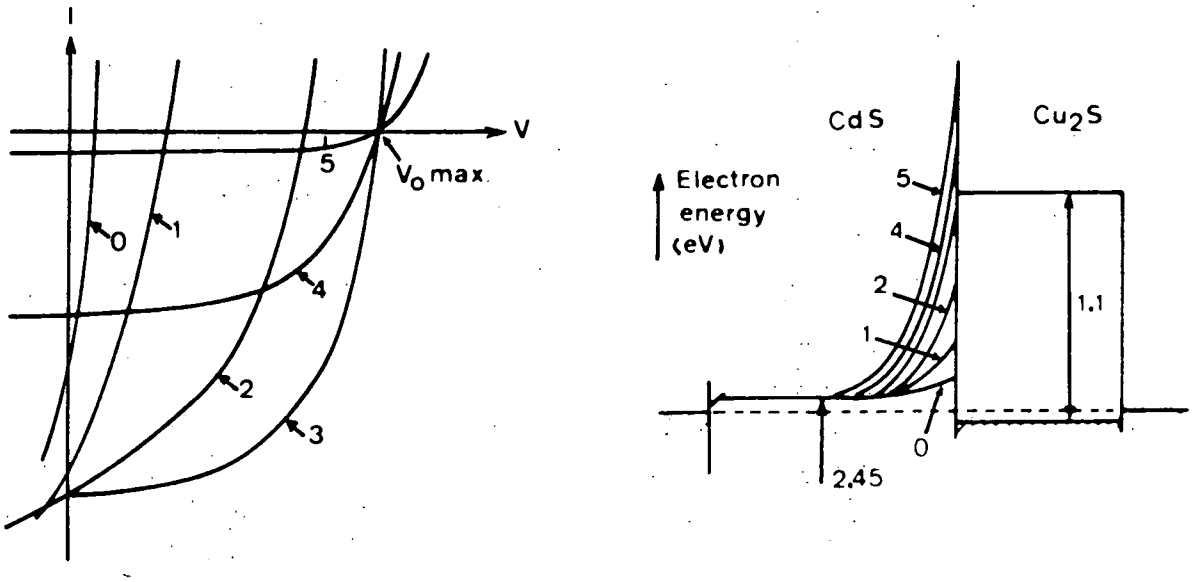


FIG. 3·8 TE VELDE MODEL . MODIFICATION OF THE I-V CHARACTERISTICS AND OF THE ENERGY BAND DIAGRAM AS A FUNCTION OF A POSTBARRIER AIRBAKE DURATION [56]

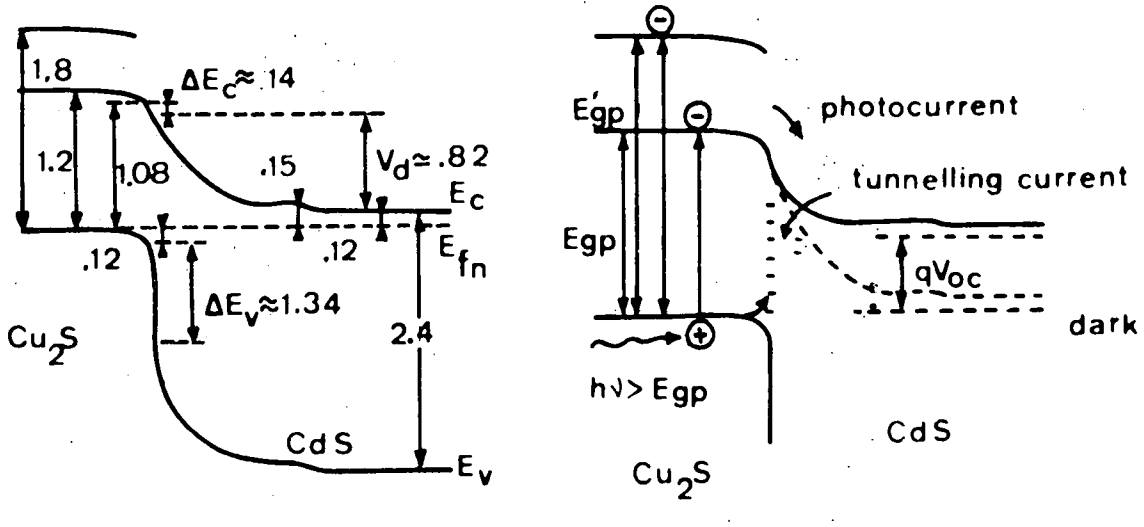


FIG. 3·9 ENERGY BAND PROFILE PROPOSED BY MARTINUZZI ET AL [59] (Energy in eV)

Böer[10, 61, 62, 63, 64, 65, 66] has considered carrier transport in CdS/Cu_2S and $(CdZn)S/Cu_2S$ heterojunction structures in great detail and has claimed a self consistent physical theory of the current-voltage relationship without invoking the superposition principle. He has analyzed the chemical and crystallographic nature of the junctions, including a consideration of the space charge double layer caused by charged dangling bonds along the dislocation network and its compensation via charge defects[64, 65]. He has concluded that the density of interface dislocations decreases when the lattice mismatch between the two component semiconductors is reduced in which case the space charge, and consequently the height of the potential spike are also decreased, with decreasing lattice mismatch: (I) a decrease in current is expected at first because of the widening of the potential spike then the current increases again as carriers move over the reduced barrier; (II) the dangling bond density and hence the interface recombination, decreases, causing V_{oc} to increase, even the height of the spike decreases. Böer has estimated the electron trap distribution from the slope and bias of non-ideal diode characteristics near the maximum power points using the kinetic method he has developed[66]. In Böer's final model[10] the photovoltaic mechanism was analysed paying special attention to the boundary conditions between emitter (light absorbed region) and junction (space charge region). Böer claimed that these boundary conditions connected the current, determined by emitter/junction boundary, with the potential drop in the junction, determined by the same conditions, and defined the current-voltage characteristic for CdS/Cu_2S and $(CdZn)S/Cu_2S$ cells which would not require the application of the superposition principle.

Partain et al[67] have suggested that a space charge limited current theory with reasonable parameters could provide a quantitative model for the gross electrical properties of CdS/Cu_2S heterojunctions left unexplained by the standard model.

Since 1976, the Institute of Energy Conversion in Delaware (USA) has consistently applied the interface recombination model to explain the behaviour of the CdS/Cu_2S cell [68] (see Fig 3.10). In this model Rothwarf[68] concluded that the simple thermal excitation model gives far too low current density and that the most probable mechanism at room temperature, near the maximum power point, is thermally activated tunnelling of electrons from the conduction band of CdS into interface states with subsequent recombination taking place close to the interface. Non-activated tunnelling of electrons and tunnelling of holes from the valence band of the copper sulphide were regarded as important only at low voltages. The model of the Delaware group has almost taken into account all the well documented phenomena such as : the large photocapacitance [69,70], the cross-over between dark and light J-V curves, infra-red quenching and enhancement effects, and time dependent phenomena all stem from changes in the space charge region of CdS related to deep hole traps ; the reversible effects on V_{OC} and J_{SC} with exposure to various ambients are associated with changes in the stoichiometry[71,72] of the thin copper sulphide layer. Recently, Rothwarf[15] has summarised the main features of the model as:

(1) In the dark the diffusion voltage in optimised cells appears exclusively in the CdS.

(2) The dominant current mechanism in the dark is via interface states at the Cu_2S/CdS junction[68]. The cross-over between J-V curves measured in the light and in the dark is due primarily to the long time it takes to establish steady state conditions in the dark. This long time constant results from the direct participation of deep levels in the CdS.

(3) Current generation in the light takes place almost exclusively in the Cu_2S layer. The magnitude of the current density J_{LO} depends on the following parameters of the Cu_2S: the thickness d ; the absorption coefficient $\alpha(\lambda)$; the electron diffusion length L_n ; the surface recombination

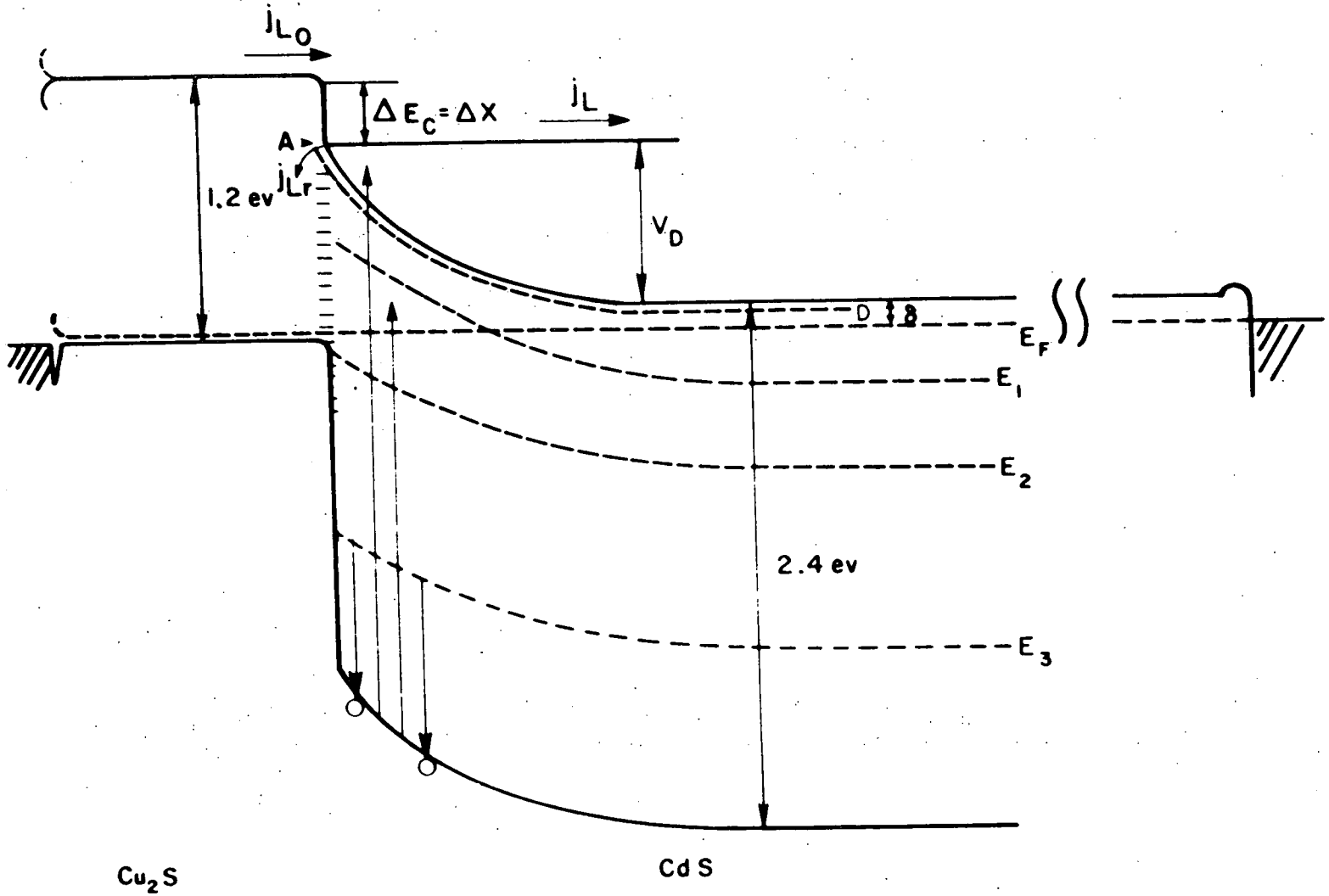


FIG. 3·10 ENERGY BAND DIAGRAM PROPOSED BY DELAWARE GROUP [68]

velocity S ; the drift field F_1 in the Cu_2S ; the radius of the grains ; the refractive index n ; the surface topology. Other factors which determine J_{LO} are the mode of operation of the cell (front-wall, or back-wall or reflection modes)[73] and the nature of the incident radiation.

(4) The short-circuit current density, J_{sc} is related to the light generated current density J_{LO} through the interface collection factor which determines the fraction of the current crossing from the Cu_2S to the CdS that reaches the contacts. The expression for the relationship is given in (3.27).

(5) F_2 is determined by the diffusion voltage V_d, the densities of shallow donors, the density and distribution of deep levels and the intensity and wavelength of the light reaching the CdS space charge region[69,74].

(6) The capacitance of the cell as a function of voltage, light intensity and heat treatment can more easily be explained in terms of the ionization of deep levels in the CdS than on the basis of a compensated region of finite extent[75,76].

(7) The general expression for the J-V relationship includes other current paths (see Fig 3.2). However the dominant interface recombination path determines the open circuit voltage[68].

With $Zn_xCd_{1-x}S/Cu_2S$ heterojunction solar cells ; Das et al.[77] proposed that the transport mechanism was interface recombination. Burton[78] has shown that the junction model is basically the same as that for CdS/Cu_2S but modified to allow for the change in the $Zn_xCd_{1-x}S$ band parameters. He concluded that the difference between CdS and $Zn_xCd_{1-x}S$ cells could be attributed to processes occurring in one or more of three cell regions : the Cu_2S, the interfacial region and the compensated region of $Zn_xCd_{1-x}S$. Oktik et al.[79] have shown that thermally activated tunnelling via interface states is the dominant carrier transport mechanism in $Zn_xCd_{1-x}S/Cu_2S$ single crystal cells.

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CHAPTER 4

EXPERIMENTAL TECHNIQUES

4.1 INTRODUCTION

This chapter is devoted to a description of the major experimental techniques and the equipment used in the present work. In the first section a brief summary of the crystal growth techniques used and the method of determining lattice parameters is given. In the following sections the fundamentals of scanning electron microscopy (SEM) and reflection electron diffraction (RED) are described. In section 4.5 and section 4.6 the equipment and experimental arrangements employed for current-voltage and spectral response measurements are summarised. Finally, a system to measure the capacitance voltage characteristics and photo-capacitance is touched on briefly in section 4.7.

4.2 CRYSTAL GROWTH

One of the typical features of II-VI compounds is that although all the elemental components have relatively low melting points, high temperatures are needed to melt the compounds. For instance, while Cd melts at 321^{o}C and S melts at 119^{o}C, the CdS compound has a melting point (under a high external gas pressure) of 1475^{o}C. At reduced pressures the compound sublimes and because of this II-VI compounds are frequently grown from the vapour phase. With this technique there are three popular methods of growing large crystals. They are :

(1) Sublimation of the actual compound.

(2) Reaction of the constituents in the vapour phase.

(3) Chemical transport using a carrier gas.

The technique, which has been used in this laboratory, is based on the sublimation method developed by Reynolds and Czyzack[1]. Piper and Polish[2] improved the technique and established a temperature gradient along the growth ampoule. Thus the material was transported from the hot to the

cooler end of the tube. The growth ampoule was then moved relative to the furnace as the crystal grew. Clark and Woods[3] modified the system by placing the unsealed growth ampoule inside an argon filled furnace tube and allowing the two tubes to communicate via a narrow opening. This method employed horizontal furnaces, which resulted in the practical difficulty of aligning the ampoule along the central axis of the growth tube. This in turn gave rise to a non-uniform radial temperature gradient which led to uncontrolled growth. To solve this problem, Clark and Woods (1968)[4] introduced a vertical system using sealed growth tubes. The experimental arrangement of this system is illustrated in Fig 4.1.

All single crystals used in this research were grown by this same technique of which the main stages are as follows :

(1) Purification of starting material : Impurities in the starting material can be very important in controlling the properties of CdS and (CdZn)S crystals. Therefore high purity commercial CdS powder (BDH Optran grade) was purified by sublimation in a continuous stream of argon[3]. The CdS powder was placed in a boat in a silica tube and maintained at 600^{o}C for four hours while a stream of high purity argon passed over it and removed volatile impurities. The temperature was then raised to 1150^{o}C to sublime the CdS which was transported to the lower temperature region of the tube leaving non-volatile impurities behind. The outcome of this process was the production of CdS platelets and rods. This process was not used with ZnS, because the temperature required was too high. Instead, ZnS starting powder (BDA Optran) was outgassed and sublimed in a continuously pumped tube.

(2) The charge (platelets for CdS and CdS platelets mixed with vacuum sublimed ZnS for (CdZn)S was loaded in the growth ampoule which was evacuated and sealed. The charge was held at 1150^{o}C in the growth ampoule which was connected via a narrow orifice to a long tail containing

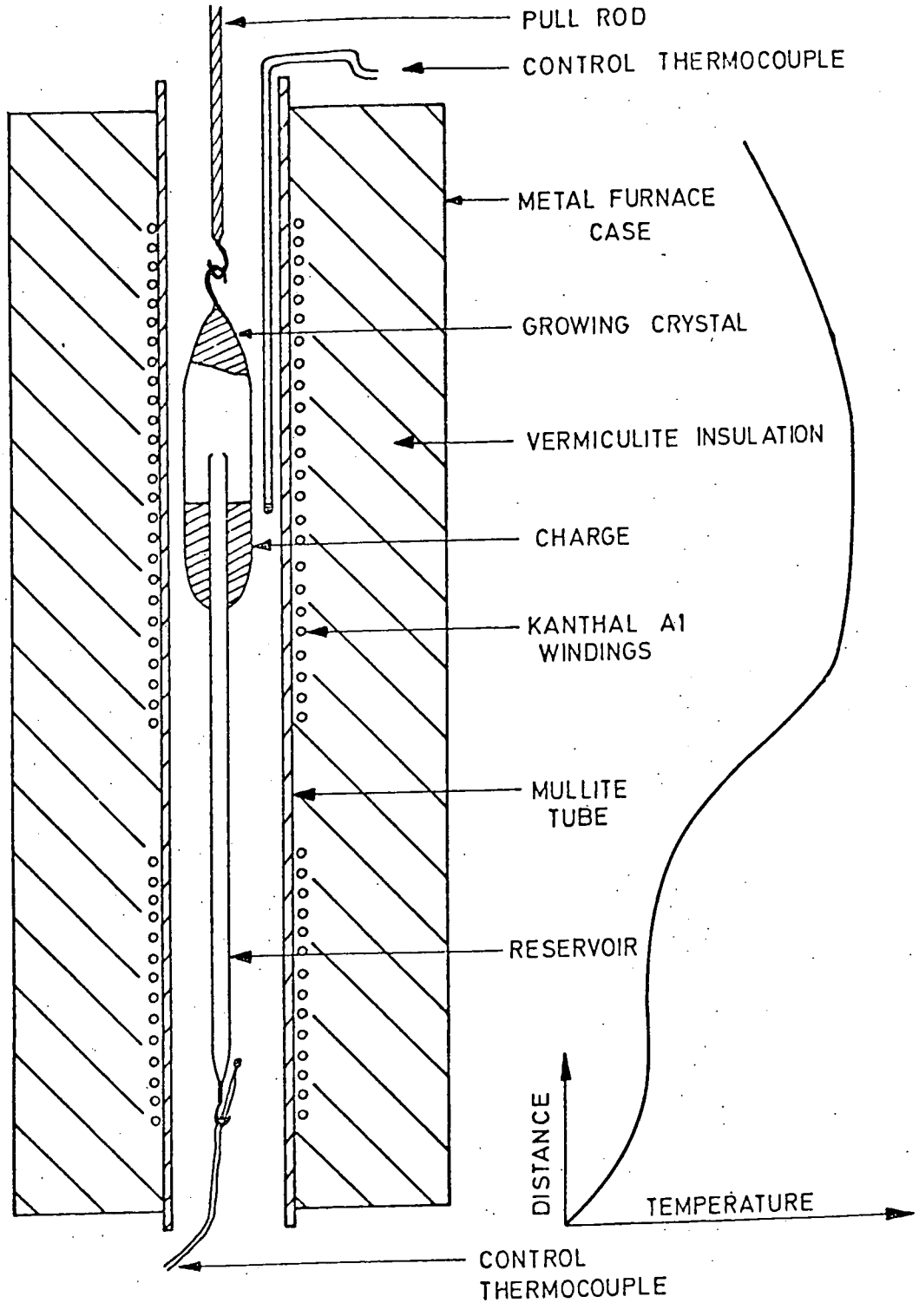

FIG. 4·1 EXPERIMENTAL ARRANGEMENT FOR THE GROWTH OF CdS AND (CdZn)S SINGLE CRYSTALS FROM THE VAPOUR PHASE

a reservoir of cadmium or sulphur. The temperature of the tail was adjusted to provide an appropriate vapour pressure over the evaporating charge. Higher reservoir temperatures were required as the zinc content increased. In fact with mixed crystals the charge was first converted to a solid solution of (CdZn)S in a reverse temperature gradient, then as the capsule was pulled and the growth gradient was developed the various vapour species diffused to the cooler regions where super-saturation occurred and crystals grew.

As is well known, the crystallites of evaporated films of CdS are columnar with their +c axes approximately perpendicular to and pointing up from the substrate [5]. Thus in order to compare cells prepared on single crystals with those prepared on thin films, devices were generally formed on the $(000\bar{1})$ planes of the single crystals. Since the growth axis of a single crystal boule did not usually coincide with the c-axis, x-ray back reflection was used to orient the boules.

4.2.1 X-ray Powder Photography

In order to determine the lattice parameters and the composition of mixed crystals, X-ray powder photographs of crushed $Zn_xCd_{1-x}S$ $(0 \lesssim x \lesssim 0.5)$ crystals were taken using 2 to 3 hours exposures. The patterns were indexed using a graphical method [7]. Since hexagonal crystals are characterised by two variable parameters a_o, and c_o, the plane spacing equation is [7]

$$\frac{1}{d_{hkl}^2} = \frac{4}{3}\,\frac{h^2 + hk + k^2}{a_o^2} + \frac{l^2}{c_o^2}$$

This equation is combined with Bragg's law $\lambda = 2\, d_{hkl} \sin\theta$ where λ has a weighted mean value of 1.5418 $\mathring{A}$ for Cu $K\alpha_1$ and Cu $K\alpha_2$ radiation, to calculate the lattice parameters a_o and c_o.

4.3 SCANNING ELECTRON MICROSCOPY

In an attempt to analyse the surface topography and examine the electrical properties of CdS/Cu_2S and (CdZn)S/Cu_2S heterojunctions on a microscopic scale, the devices were studied in a Cambridge Stereoscan 600 scanning electron microscope (SEM). The basic components of the SEM are shown in Fig 4.2 schematically which are the lens systems, an electron gun, electron collectors, visual and recording cathode ray tubes (CRT's) and the associated electronics. The SEM may be used in several different modes where the signals derived from the different interactions between the electron beam and a specimen are collected and used to form an image. The various interactions are summarised in Fig 4.3 and details can be found in Refs (8) and (9).

Most of our work was done in the secondary emission (SE) mode in which the secondary electrons emitted from the specimen surface were collected by an Everhart-Thornley (ET) detector consisting of a scintillator and photomultiplier. The low energy secondary electrons are not sufficiently energetic to excite the scintillator. In order to accelerate these electrons, therefore, the scintillator was held at a potential of about +14 kV, and to protect the incident beam from the influence of the high scintillator surface potential, the scintillator was surrounded by a Faraday cage which could be biased either 250V positive to collect the primary back reflected and secondary electrons, or 250V negative to collect the primary electrons only. In our work, the Faraday cage was held at +250 V in the investigation of topographic contrast. The scintillations produced by accelerated secondaries are transported via light pipe to the cathode of the photomultiplier to initiate a cascade of electrons. In this way a very large gain with very little noise is obtained.

Secondary electrons can only escape from a depth of less than 100 Å for most materials. In such a thickness most of the electrons may be assumed to be travelling nearly parallel to the incident beam direction, so that as

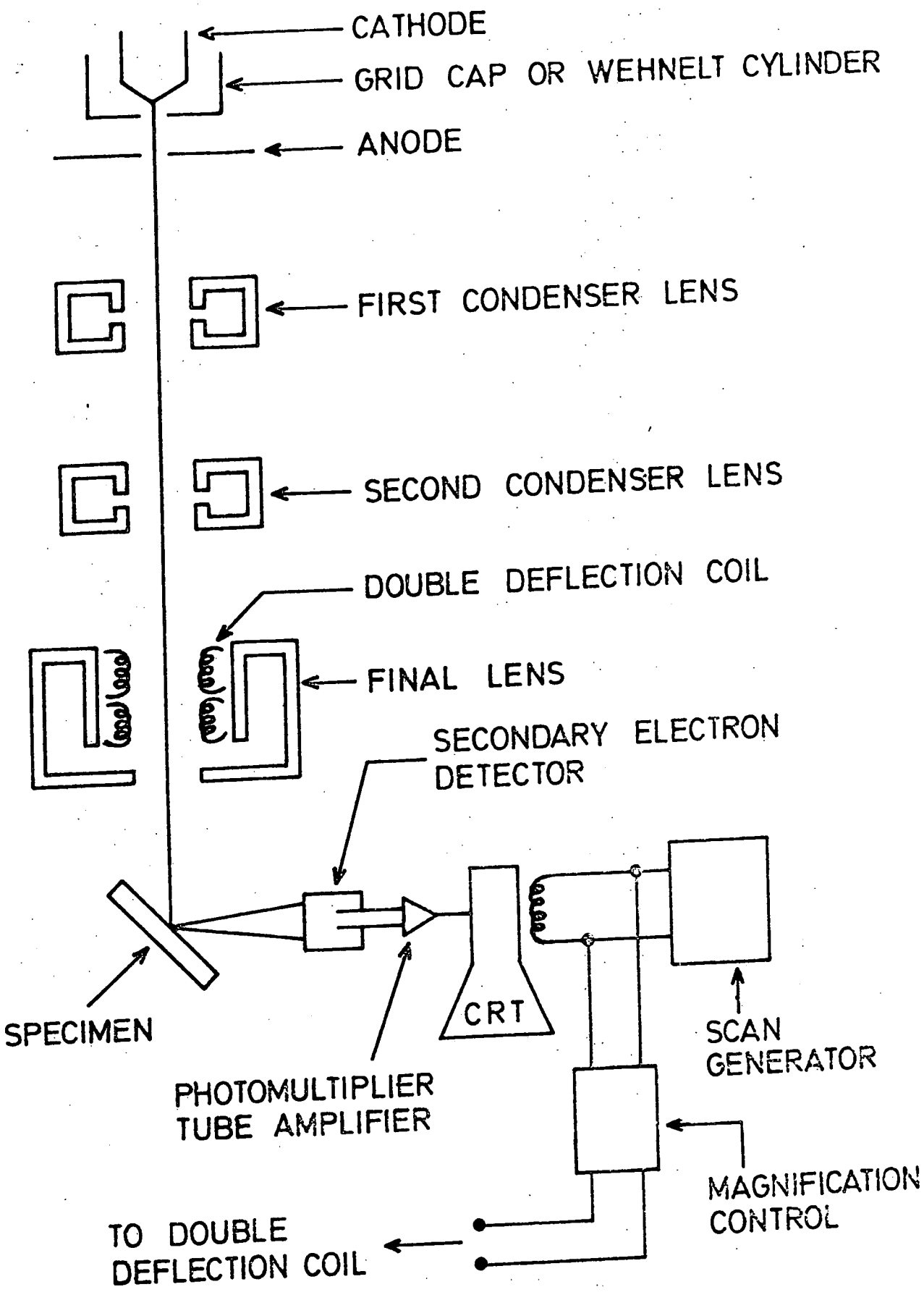

FIG. 4·2 SCHEMATIC DIAGRAM OF THE SCANNING ELECTRON MICROSCOPE

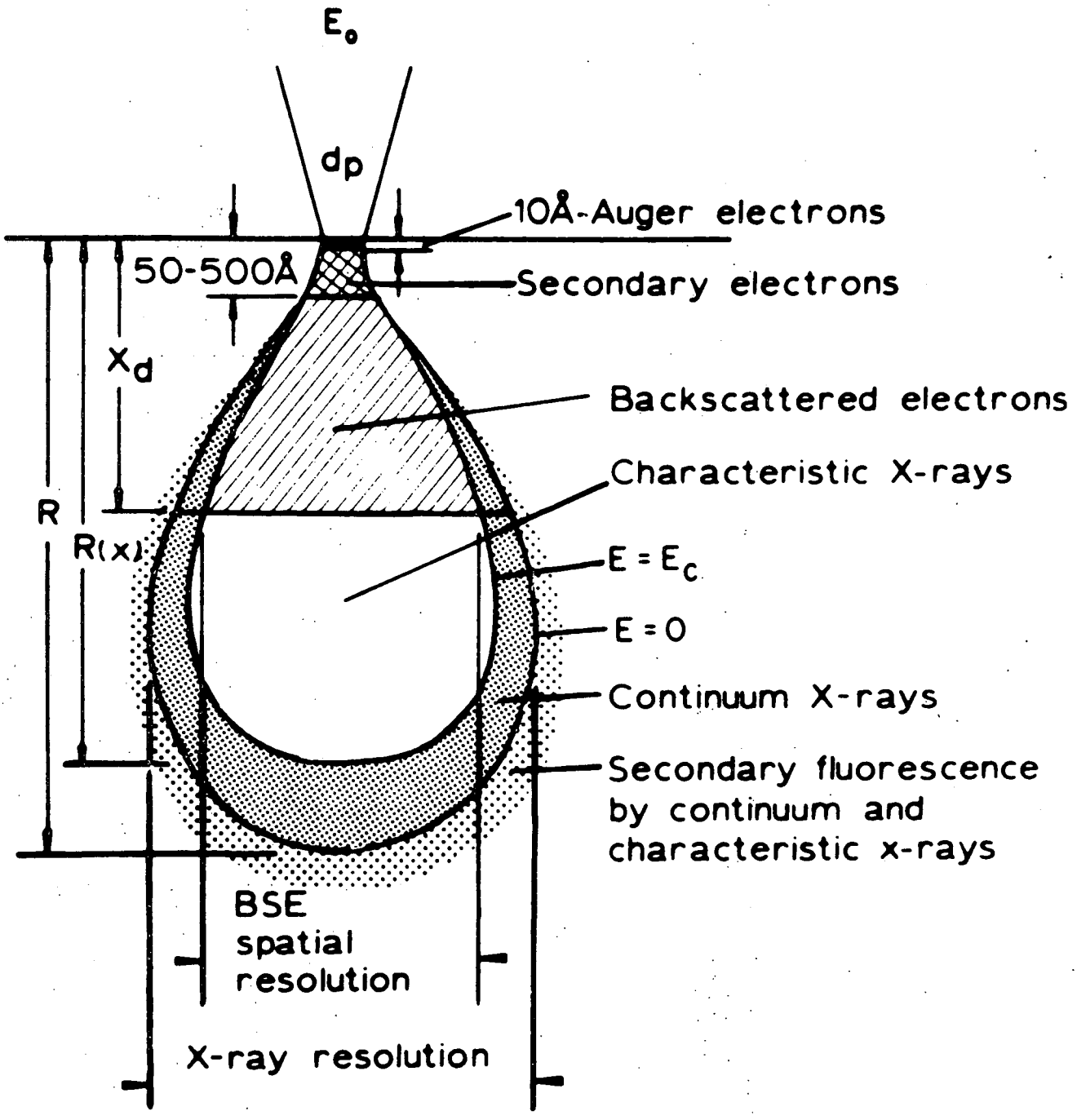

FIG. 4·3 SUMMARY OF RANGE AND SPATIAL RESOLUTION OF VARIOUS SIGNALS FROM THE ELECTRON MICROPROBE - SCANNING ELECTRON MICROSCOPE, REF [9]

the specimen is tilted away from normal incidence, the length of the beam path which lies within 100 Å of the surface increases. Consequently, the secondary electron coefficient increases markedly as a function of increasing angle of tilt. Thus a sample with facetted features will provide a good SE image because the facets are tilted at various angles to the incident beam. One of the most interesting aspects of SE images of rough samples is their direct resemblance to the same sample illuminated by light and viewed optically. A detailed discussion of image formation in the SEM may be found in several texts (see for instance the books by Holt et al [8] and Goldstein et al [9]).

One of the SEM modes heavily used in this study was the Electron Beam Induced Current (EBIC) mode, salient features of which are described in Chapter 6.

4.4 REFLECTION ELECTRON DIFFRACTION (RED)

The reflection electron diffraction studies were carried out in a JEM 120 transmission electron microscope (TEM). The RED technique provides information about surface films, surface perfection, crystal structure, the degree of preferred orientation of crystallites at the surface etc., The technique is easy to apply and observations are straightforward to interpret.

In RED an electron beam with energy in the range of 10 to 100 keV produces diffraction effects from atomic planes at the surface of crystalline specimens. If the Bragg diffraction requirement is fulfilled

$$\lambda = 2d_{hkl} \sin\Theta \qquad (4.1)$$

where the wavelength, λ, depends on the accelerating voltage and varies from 0.12 to 0.04 Å in the energy range from 10 to 100 keV, d_{hkl} is the interplanar spacing and Θ is the angle between the beam and the atomic planes (the Bragg angle). A typical interplanar spacing is of the order

of Angstroms (Å), so that to obtain a diffraction pattern the Bragg angle varies between 1.5° and 0.5°. Consequently, in the RED technique only those crystal planes that are inclined at less than a few degrees to the surface of a specimen will diffract an electron beam. The conditions necessary to produce an electron diffraction pattern are illustrated in Fig 4.4. Each plane (hkl) in real space produces a reciprocal lattice point (the reciprocal lattice point lies on a line perpendicular to the real space planes) if the incident beam is incident at the Bragg angle (θ) then a diffraction spot is formed on the fluorescent screen placed at a distance, L, from the sample. In three dimensions the Bragg reflection condition may be determined using a geometrical model known as the Ewald sphere construction (Fig 4.5). In this graphical representation of Bragg's law of diffraction, constructive interference arises only if the reflection sphere intersects a point in the reciprocal lattice (point B). As the radius of this sphere is $1/\lambda$, it is very large compared with the reciprocal lattice distances of $1/d_{hkl}$ for the diffraction of a beam of high energy electrons, and the sphere may be approximated to a plane section through the reciprocal lattice. Therefore the RED pattern observed corresponds to the plane section of the reciprocal lattice which lies perpendicular to the direction of the incident beam.

The usefulness and advantages of RED compared with X-ray techniques are as follows (Russell [10]).

(i) In forming a diffraction pattern, the beam penetrates a much smaller volume of material (the depth of penetration of an electron beam at glancing incidence is only of the order of 100 Å for very smooth surfaces, (although it is deeper for rough surfaces).

(ii) Changes in the complete diffraction pattern may be clearly observed on a fluorescent screen as the crystal orientation and diffraction condition are varied.

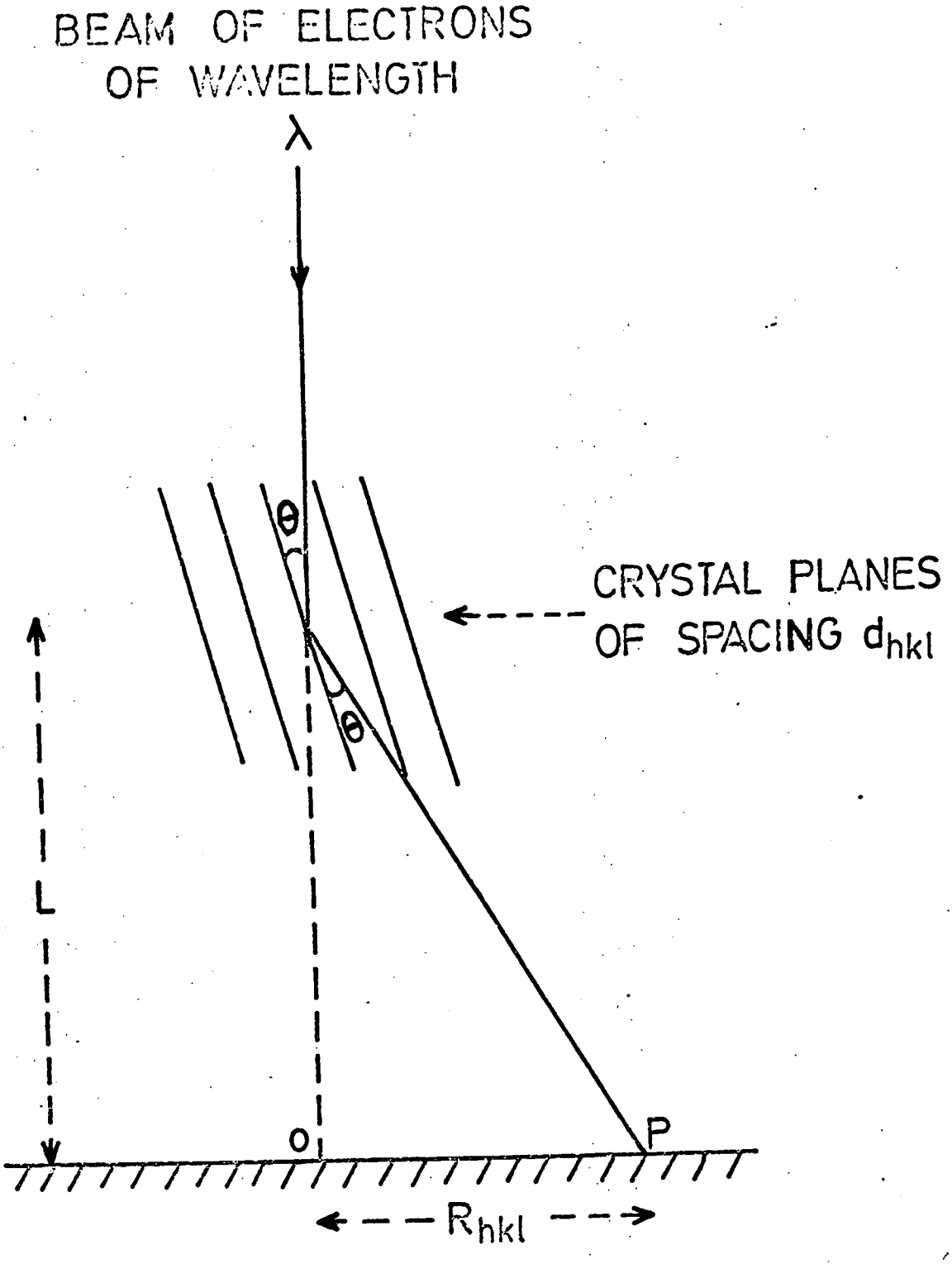

FIG. 4·4 SCHEMATIC DIAGRAM OF REFLECTED ELECTRON DIFFRACTION

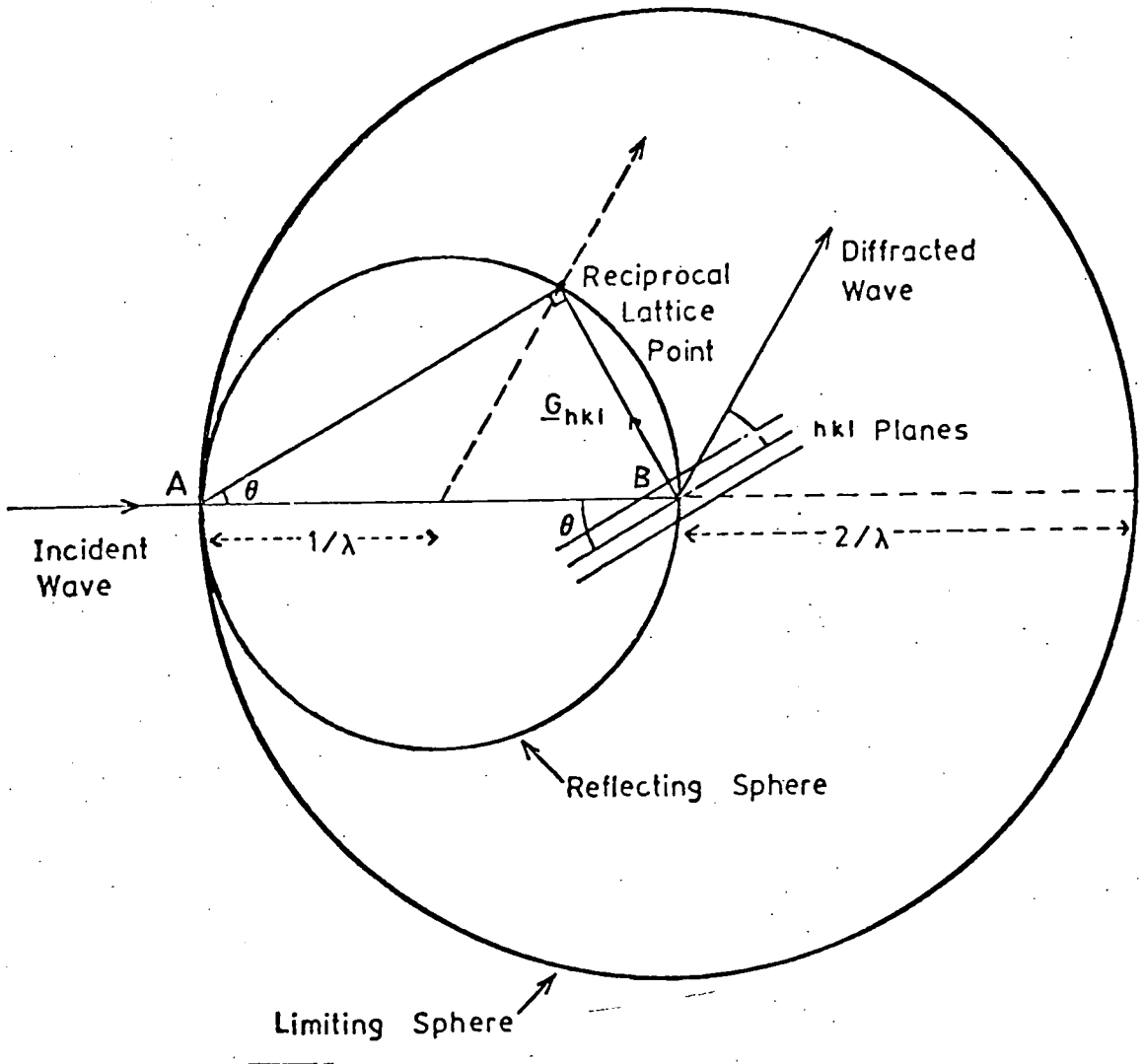

FIG. 4·5 SPHERE OF REFLECTION IN A RECIPROCAL LATTICE

(iii) For the photographic recording of RED patterns the exposure time is typically of the order of seconds, for X-rays it can be several tens of minutes.

(iv) As the Bragg angle for RED is so small ($\sim 1^{o}$) a pattern covering a large number of reflections in reciprocal space can be recorded on a flat photographic film (with X-rays a large angular spread of patterns has to be covered).

(v) Because the planes in real space lie approximately parallel to the incident beam it is easier to visualise the transformation from real to reciprocal space.

Examination of diffraction patterns from real space planes enables lattice parameters to be calculated using the camera equation for the microscope ($\lambda L = R_{hkl} d_{hkl}$ [10]). However, certain crystal orientations give rise to standard, easily recognisable patterns which provide clear information about the structure at the surface. In the present work the RED technique was heavily used to identify both the crystal structure of polished and etched CdS and (CdZn)S surfaces prior to the chemiplating process, and the phase of the copper sulphide layers formed on these surfaces after chemiplating.

4.5 MEASUREMENT OF CURRENT-VOLTAGE CHARACTERISTICS

Current-voltage characteristics were recorded in the dark at different temperatures, and under AM1 illumination at room temperature. Simulation of AM1 illumination was accomplished using 1.5 kW quartz-halogen strip lamp with a parabolic reflector housing, and a 2 cm deep tray of flowing water as a filter which reduced the infrared content. The source was calibrated using a standard silicon PIN diode (type 10 DF, United Detector Technology) and adjusting the distance between source and sample. Measurement of the current-voltage characteristics were carried out point by point using a high impedance Bradley voltmeter (type 173B)

for voltage readings, and a low impedance Hewlett Packard amperemeter (type 3465B) for current readings. In addition to this an automatic current-voltage tracer was also used to monitor the changes in the device characteristics. During the measurements the cell was maintained in a vacuum. Temperature dependence of current-voltage characteristics was studied using a cryostat, the main parts of which are shown in Fig 4.6. The unit was designed around a 2 cm i.d. gas exchange vessel. This is connected to a copper specimen block fitted with a heater at one end and to the liquid nitrogen container about 1 litre capacity at the other. The pressure in the cryostat was maintained well below 10^{-3} torr by an Edwards 11cc oil diffusion pump. Thermal conduction between the copper heat exchanger block and the liquid nitrogen container was adjusted by varying the pressure of the gas in the exchange vessel. Variable temperatures were obtained by balancing the low temperatures provided by liquid nitrogen and the heat provided by the heater on the heat exchange block. The temperature of the specimen was monitored using a copper-constantan thermocouple placed in close proximity to the sample. All necessary electrical contacts for measurements were made through 8 way glass-metal seals at the top of the cryostat.

4.6 MEASUREMENT OF SPECTRAL RESPONSE

The response of cells was recorded over a wavelength range from 0.4 to 2.0 μm using a "Barr and Stroud" double prism monochromator, type VL2, fitted with a Spectrosil 'A' silica prism. A 250 watt 24 volt quartz-halogen lamp driven by a d.c. stabilised power supply was used as the light source. The energy distribution of the source at the exit slit, which includes the varying dispersion of the prism monochromator was measured using a thermopile with a combination of light chopper and lock-in amplifier. The light was chopped at a frequency of 10 Hz. In addition an accurate recording of the spectral distribution of energy at the exit slit over the wavelengths $0.45 < \lambda < 0.95$ μm was made using the silicon PIN diode

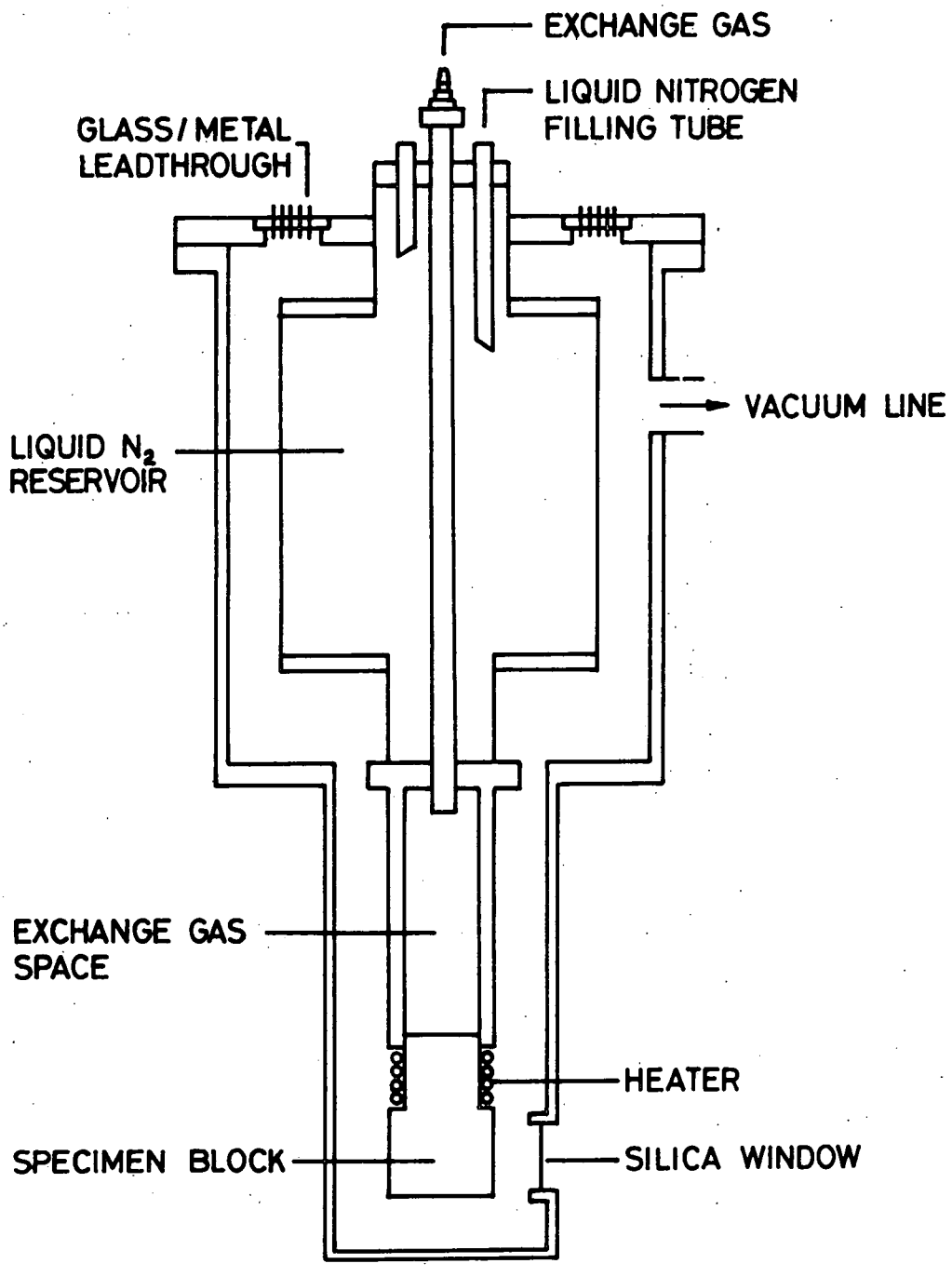

FIG. 4·6 CRYOSTAT

(type 10 DF). The distributions measured with both detectors were almost identical, Fig 4.7. In order to avoid the effects of wavelength drift in the monochromator, the calibration procedure was repeated using a sodium source. Throughout the work the width of the entrance and exit slits was adjusted to 0.5 μm. The device under test was mounted in a cryostat which had the facility of a second window for secondary illumination. The cell was always illuminated from the front (front-wall mode), and the temperature was monitored. The photovoltaic current and voltage were measured using a Keithley Electrometer Model 602 which has an input impedance of 10^{14} ohms for voltage measurements and very low input impedance for current measurements. Thus, recorded V_{OC} and I_{SC} spectra are adequate approximations to the open circuit-voltage and short circuit current conditions. The output of the electrometer was traced by a Honeywell Electronic (Model 196) high impedance chart recorder. A block diagram of measurement system is shown schematically in Fig 4.8.

4.7 MEASUREMENT OF JUNCTION CAPACITANCE

The junction capacitance of the CdS/Cu_2S and $(CdZn)S/Cu_2S$ devices was measured as a function of bias voltage and the wavelength of the incident light using a phase-sensitive detection technique. A Brookdeal "Ortholoc" model 9502 was used for all these measurements. A block diagram of the circuit arrangement is shown in Fig 4.9. The reference signal with a frequency of 100 KHz and a peak-to-peak voltage of 20 mV was provided by a Brookdeal 5012F oscillator. The circuit shown in Fig 4.9 was designed to measure the capacitance and conductance at high frequencies. To be able to measure the correct value of capacitance and conductance with this arrangement the conditions given below have to be fulfilled

$$R_L << 1/G_x \quad \text{and} \quad R_L \omega^2 C_x << G_x$$

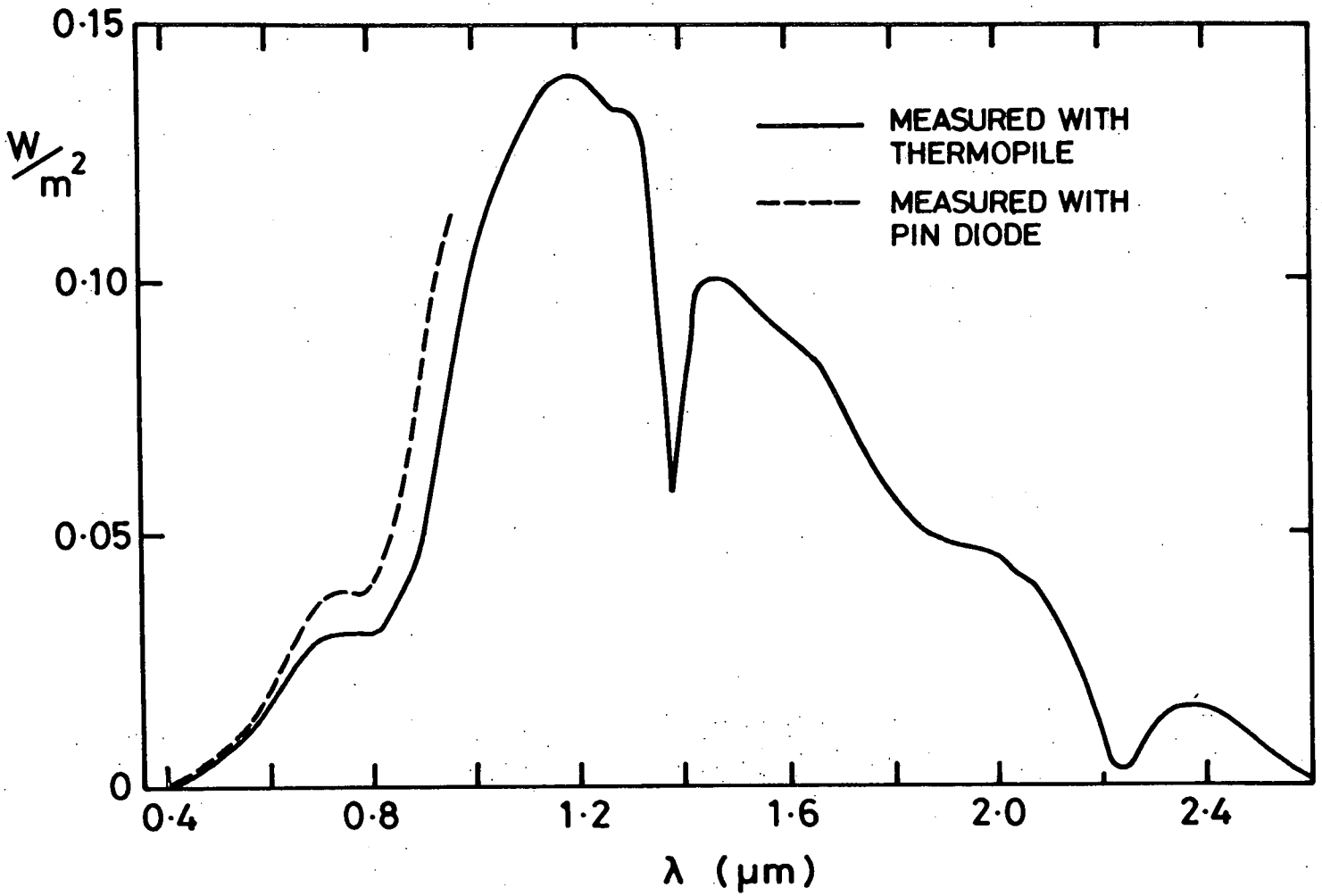

FIG. 4·7 ENERGY DISTRIBUTION OF LIGHT SOURCE AND MONOCHROMATOR

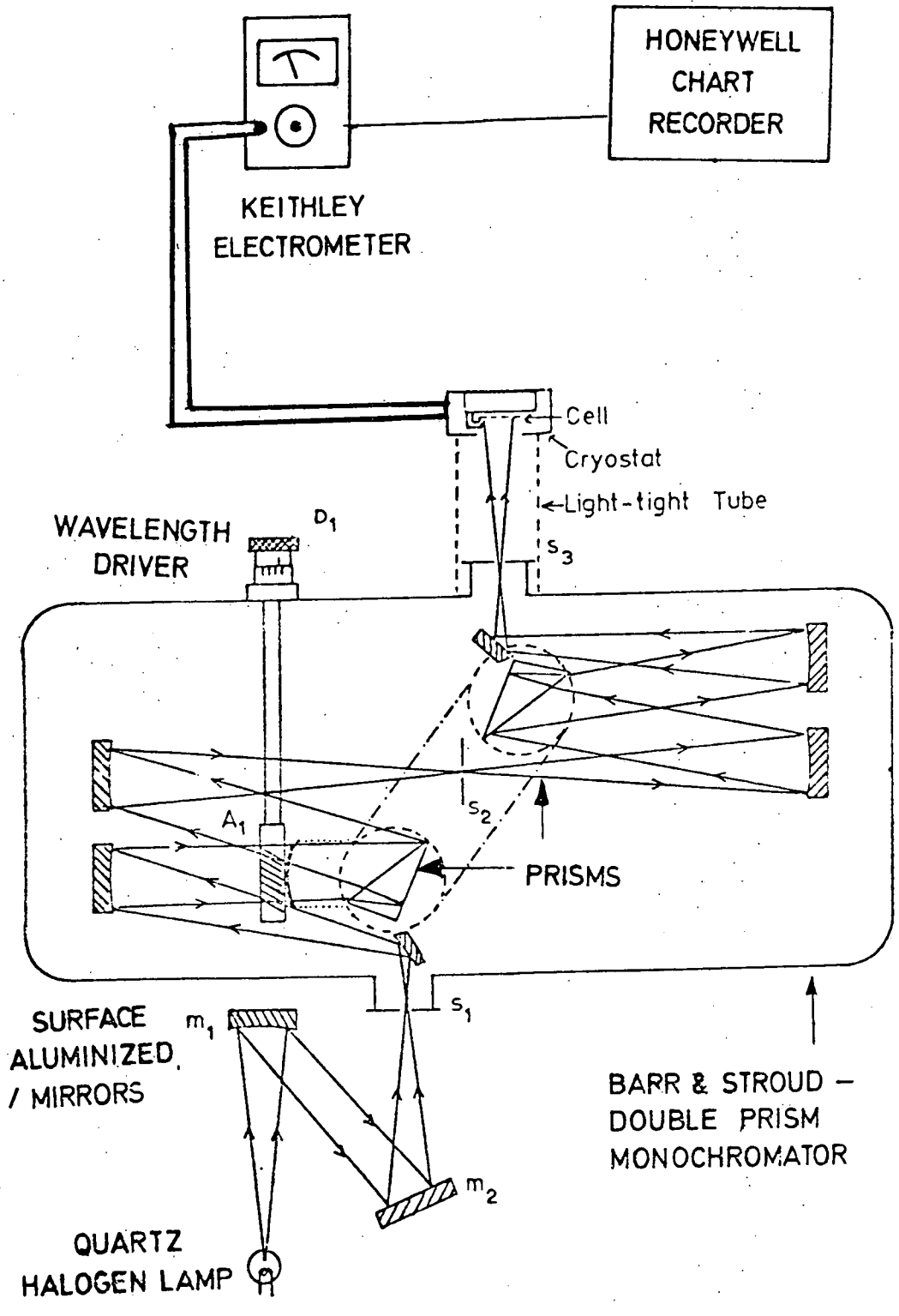

FIG. 4·8 EXPERIMENTAL SET UP USED FOR PHOTORESPONSE MEASUREMENTS

then the voltage across R_L is given by

$$V_L = V_s R_L (G_x + j \omega C_x)$$

This can be represented by two voltages, one in phase with the signal voltage, V_s, namely $V_s R_L G_x$, and the other in quadrature with V_s, namely $V_s R_L \omega C_x$. Thus both voltages can be measured simultaneously using a two channel phase sensitive detector to provide information about the conductance and capacitance. These measurements were made in both forward and reverse bias using an integrated circuit voltage ramp with a scan rate adjustable from 1 sec/volt to 1000 sec/volt. The ramp voltage was fed directly to the x-input of a Hewlett Packard X-Y-T recorder model 7041 A, and either the in-phase or quadrature output was fed to the Y-input to display C-V and G-V characteristics.

Before every measurement, the system was calibrated using standard silver-mica capacitors and the following procedure; the capacitance of the device was roughly estimated and the nearest available standard capacitor was connected across the test points. Next, the Ortholoc phase control was adjusted until the in-phase component (conductance) read zero, and then the device capacitance and conductance values were compared with this.

4.7.1 Infrared Quenching of Photocapacitance

A technique in which photocapacitance spectra are recorded with the device under continuous bias illumination, allows the rapid characterisation of deep-traps in a semiconductor. A comprehensive discussion of the technique can be found in the report by Sah et al (11).

In our work the steady level of bias light corresponding to the fundamental absorption edge of CdS was obtained by filtering the light from the quartz-halogen source with an Oriel 5200 band pass and infrared absorption filter. This excitation served to create a steady population of holes in levels below the Fermi level of the CdS and electrons in

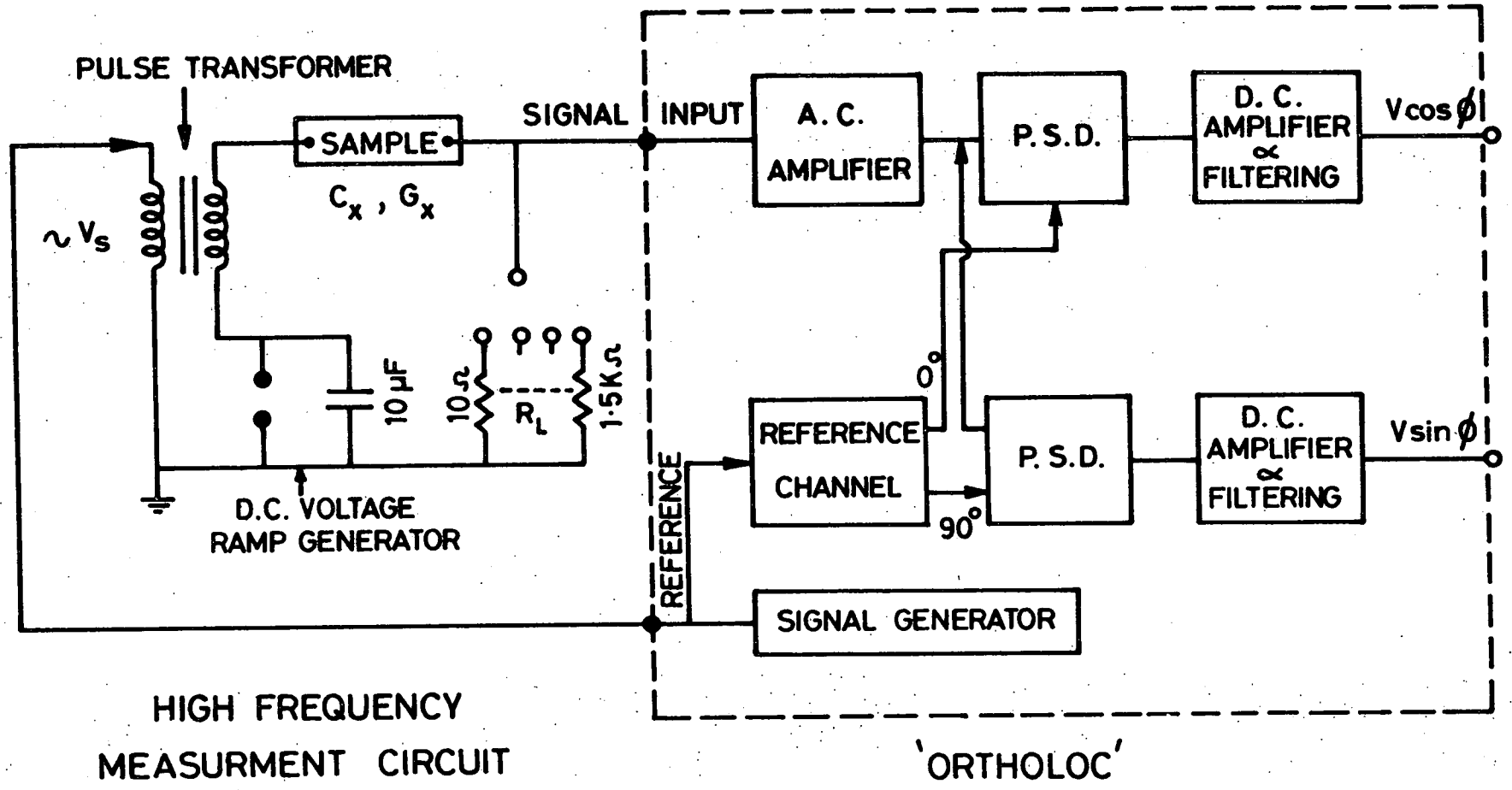

FIG. 4·9 BLOCK DIAGRAM OF PHASE SENSITIVE DETECTION TECHNIQUE.

trapping centres above it. Thus as the monochromatic probe illumination was scanned from a wavelength of 2 μm to 0.4 μm, the probe light upset this population by the excitation of electrons from the valence band into hole traps, or of electrons from the levels above the Fermi level into the conduction band. As a result, the space charge distribution was altered, and the capacitance changed to a new value which was greater or lower according to the nature of the transition involved. The superiority of the photocapacitance technique when compared with that of photoconductivity is that it can be applied to low resistivity samples and also determines whether electron or hole traps are involved.

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CHAPTER 5

ANALYSIS OF CdS/Cu_2S SINGLE CRYSTAL PHOTOVOLTAIC CELLS

5.1 INTRODUCTION

The results to be described in this chapter show that CdS/Cu_2S photovoltaic cells on single crystal substrates can be prepared with optimum efficiency in their as-plated state provided that they are produced under suitable conditions in which the surface preparation, the bulk resistivity of CdS and the stoichiometry of Cu_xS are properly controlled. In an attempt to optimize the parameters involved, the various stages in the preparation of cellshave been extensively investigated and ultimate behaviour of the devices has been correlated with different aspects of the preparative procedures. In section 5.2 studies of the surface treatment prior to the formation of the copper sulphide have been made, using the techniques of reflection electron diffraction (RED) and scanning electron microscopy (SEM), and the surfaces are classified according to the treatment given. The following section is concerned with the work on the modification of the chemiplating technique and the formation of Cu_xS, as it controls the phase and the thickness of the layer. Once again the SEM and TEM were the main tools employed. Sections 5.4 and 5.5 are devoted to the evaluation of devices fabricated under different conditions in their as-made state. Current-voltage characteristics were measured in the dark and under air-mass one (AM1) illumination and the spectral distribution of V_{oc} and I_{sc} were also determined. Further, the operational parameters of the cell have been analyzed and related to the preparative parameters. Finally, in section 5.6 the effects of a post barrier air-bake on differently classified devices are described in some detail.

5.2 STRUCTURE OF POLISHED AND ETCHED $(000\bar{1})$ CdS SURFACES

The devices used were fabricated on dice with dimensions of 4x4x2 mm^3 cut from large single crystals of CdS grown in this laboratory using the technique described in chapter 4, section 4.2. The single crystal boules were first oriented using X-ray back reflection techniques and then cut into slices 2 mm thick with the c-axis perpendicular to the large area faces. Sawing with the diamond wheel leaves the slice with severely work damaged surfaces. Chemical etching of these surfaces to remove the work damaged layer resulted in very rough surfaces with numerous large hillocks, steps and kink sites. In order to remove saw marks and produce physically smooth surfaces before the chemical etch was administered, some of the slices were polished, by hand on a polishing pad, or on a lapping wheel using alumina powder of different particle sizes. They were then cut into dice. Other slices were cut into dice first before being polished. The CdS single crystals were entirely hexagonal as grown (RED examination). However the mechanical polishing of surfaces obviously disturbs the hexagonal structure of CdS single crystal, Fig 5.1 shows the reflection electron diffraction (RED) pattern from a CdS surface after mechanically polishing it with 1 μm alumina powder. The diffraction rings in this pattern indicate the existence of a polycrystalline layer of CdS on the surface. Inspection of the relative radii of the first three rings shows they increase in the sequence $\sqrt{3}$, $\sqrt{8}$, $\sqrt{11}$ and are indexed as the (111), (220) and (311) reflections of the cubic sphalerite phase of CdS[1] A similar cubic polycrystalline surface layer is produced on single crystals of CdSe and ZnS by mechanical polishing[1]. When the surfaces of single crystal CdS were polished with alumina of particle size greater than 5 μm the same phase transformation to sphalerite cubic was observed, but additional diffraction rings were present in the RED pattern obtained from these samples and these were indexed as arising from α-alumina, Fig 5.2. In fact this observed phase transformation from wurtzite to sphalerite is a well known effect of grinding or ball-milling hexagonal

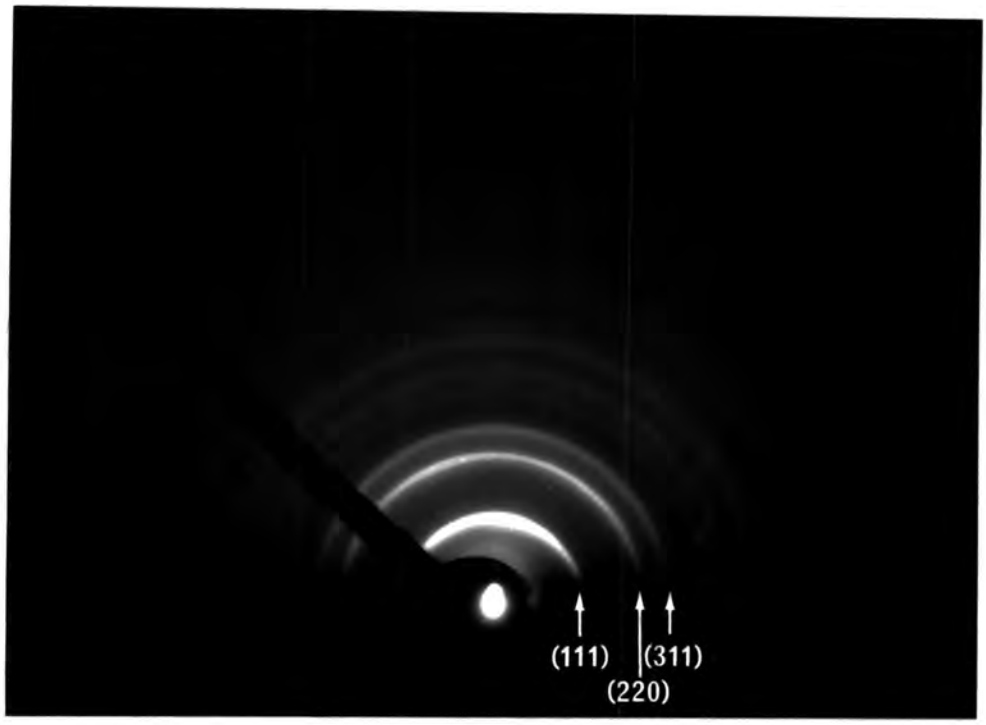


Fig 5.1: RED pattern from CdS surface after polishing with alumina powder of 1 μm particle size.

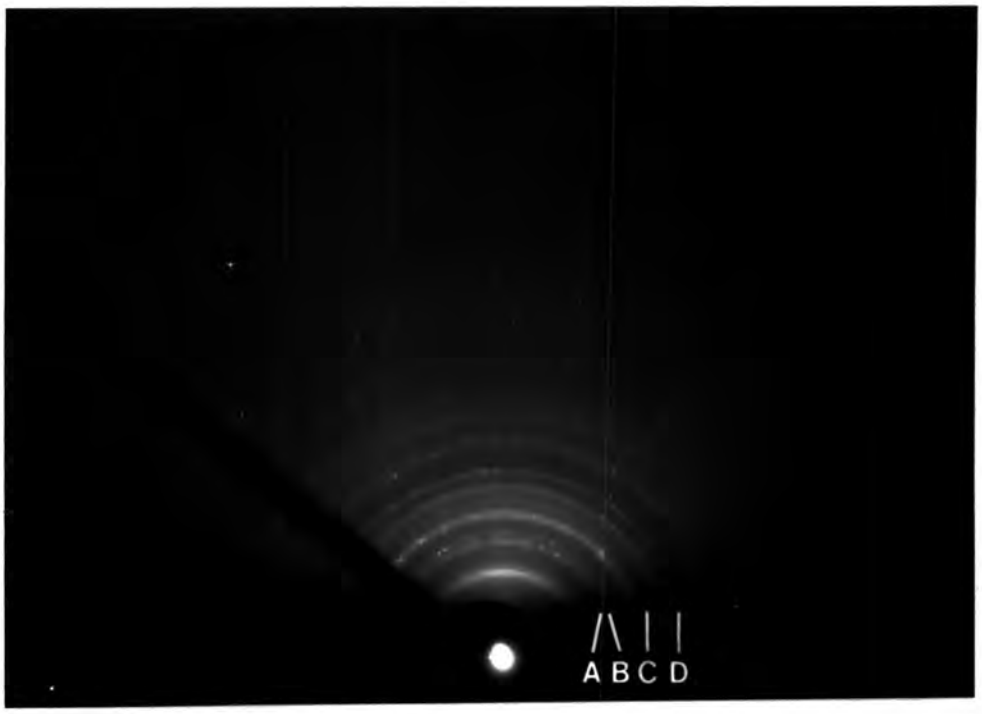


Fig 5.2: RED pattern from CdS surface after polishing with alumina powder of 5 μm particle size.

phosphor powders and was first reported in 1948[2].

In general, during the fabrication of CdS cells the CdS is usually etched prior to junction formation. Although a number of etchants have been examined in this work (such as H_2SO_4, solutions of Cr_2O_3 in H_2SO_4,HF), the use of a concentrated HCl etch was found to be the best for producing high performance cells.

The etching of CdS single crystal dice in HCl enabled the two polar surfaces to be distinguished[3]. Etching,therefore, was a very important stage of cell fabrication, not only for the identification of polar surfaces but also for the removal of the polycrystalline layer on the surface. After etching for a few seconds the RED pattern shown in Fig 5.3 was obtained. It shows features from both the polycrystalline layer and the underlying hexagonal single crystal. In addition, there are arcs of intensity passing through many of the diffraction spots of the hexagonal structure. In fact, the SEM examination (in the SE mode) of the surfaces of samples etched for less than 5s.indicated that they still exhibited evidence of damaged surface regions (see Fig 5.7). However, by extending the etching period ($\sim$ 20s) a hexagonal single crystal pattern of CdS could be obtained, Fig 5.4.

SEM examination showed that etching of the mechanically polished sulphur face $(000\bar{1})$ of CdS always produced etch hillocks on this plane. However, topographic features of these hillocks were found to be related to the type of surface treatment which had been given prior to etching. Hereafter the samples, cut from slices which were mechanically polished by hand will be called type A dice, and those first cut into dice from unpolished slices then hand polished will be called type B dice. Comparison of Figs 5.5 and 5.6 demonstrates the differences in the surface topography of hillocks on type A and type B surfaces which have been mechanically polished with 1 μm alumina powder and then etched for 30 s in concentrated HCl. Other samples polished on a lapping machine as a group of slices or dice using alumina of

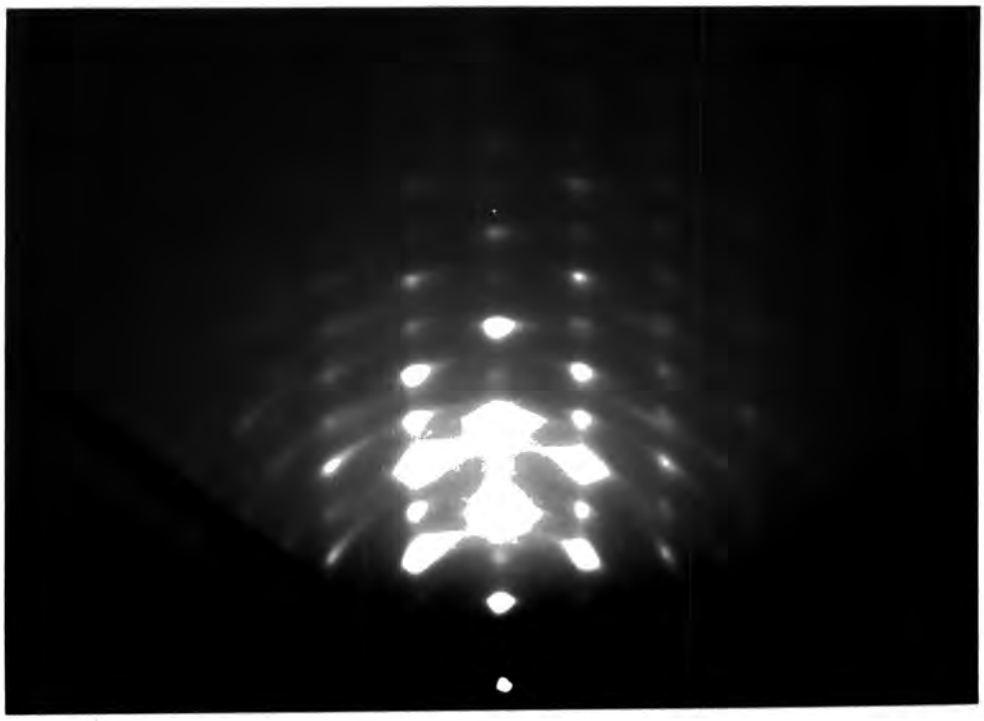


Fig 5.3: RED pattern from a mechanically polished surface after etching it in concentrated HCl for a short time (< 2s).

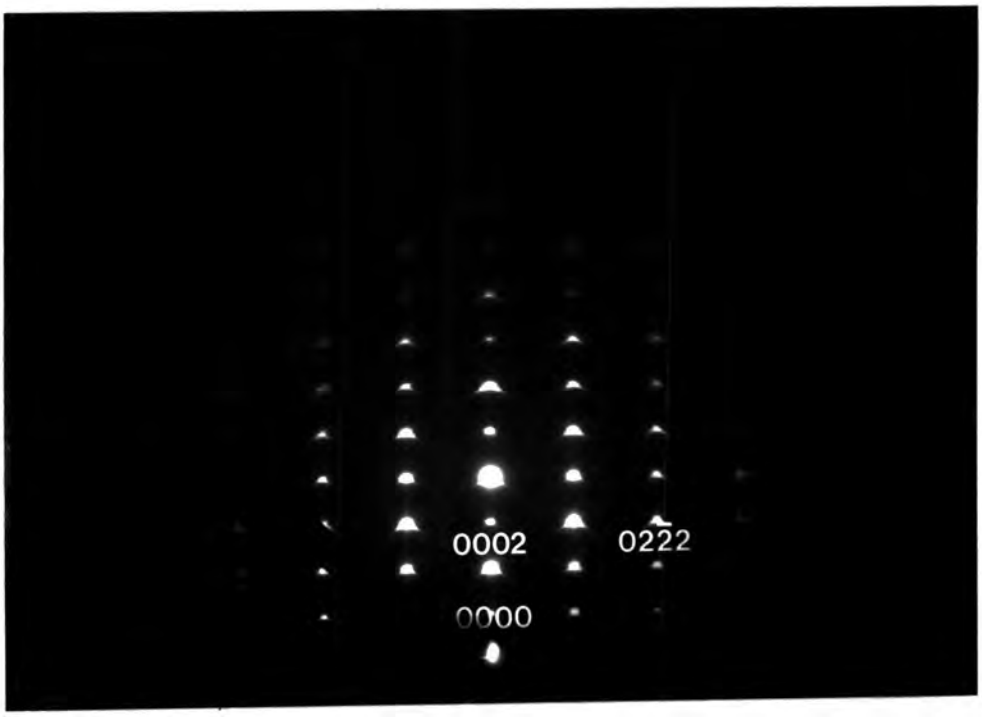


Fig 5.4: RED pattern from a mechanically polished CdS surface after etching it in concentrated HCl for 30s.

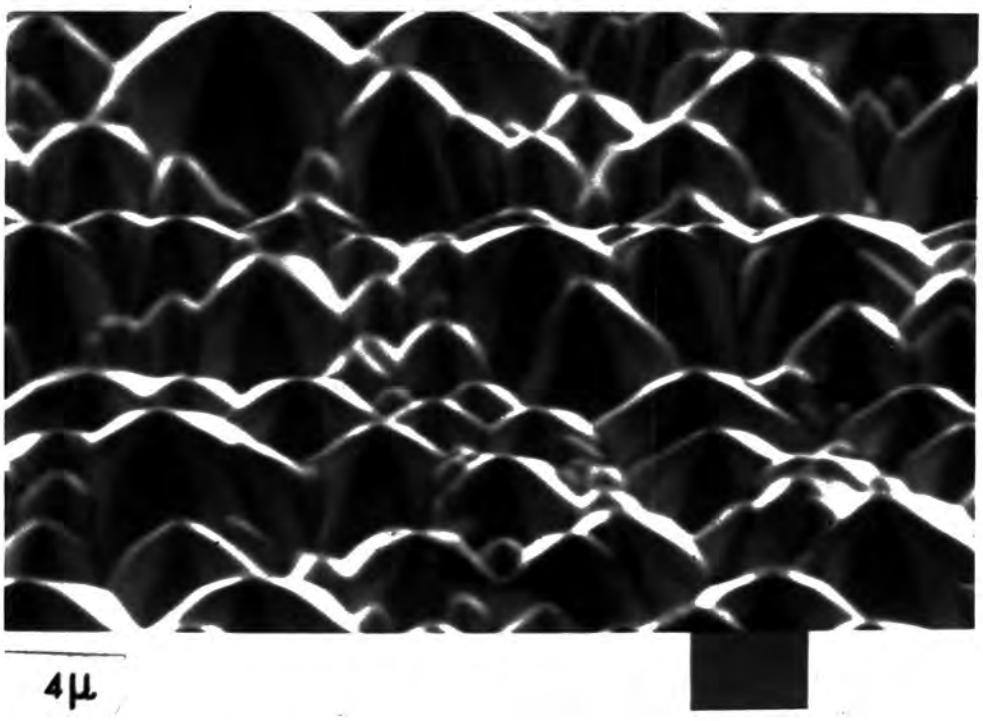


Fig 5.5: Secondary Emission micrograph of CdS type A surface etched in concentrated HCl for 30 s.

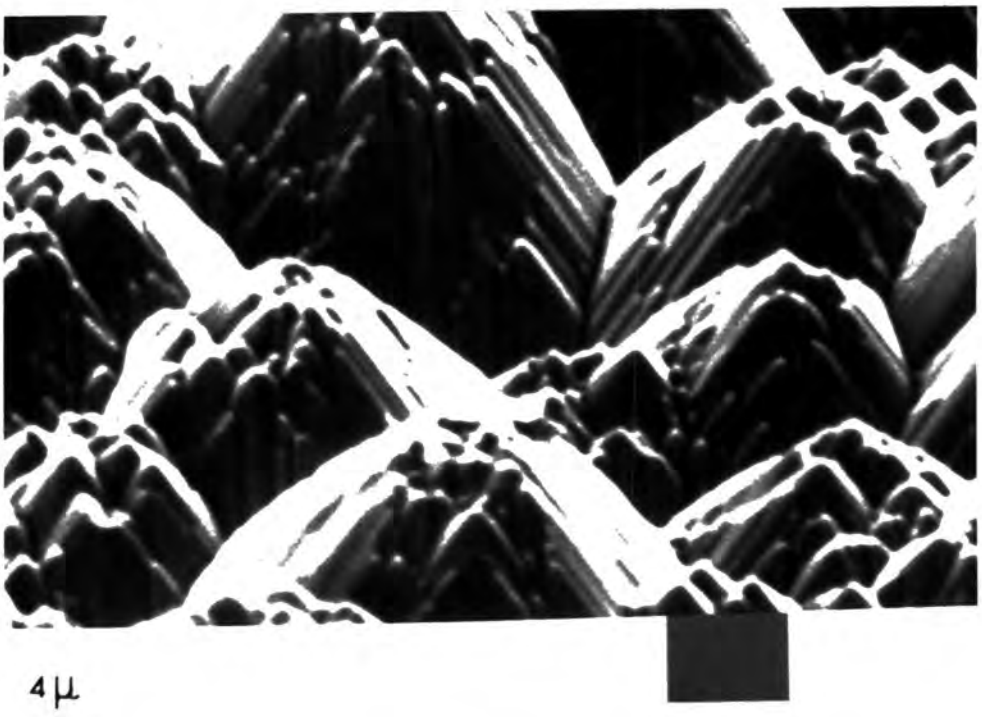


Fig 5.6: Secondary Emission micrograph of CdS type B surface etched in concentrated HCl for 30 s.

1 μm particle size appeared to have a similar surface topography to that shown in Fig 5.5.

In order to determine the relative effects which the etching period and particle size of the alumina had on the etch pattern, the samples were polished with alumina of 1 and 5 μm particle size (as in type A preparation) and then etched for 5 s, 15 s, 30 s, and 60 s in concentrated HCl at room temperature. In Fig 5.7 (a) and (b), the resulting SE micrographs show the relative development of etch hillocks. Extending the etching period on both samples polished with 1 and 5 μm alumina results in larger hillocks on the surface. However, a similar etching period gives rise to a larger hillock size on the surface polished with 5 μm particles of alumina, Fig 5.7 (b). When the hillocks increased in size, ledges and kink sites developed simultaneously on their sides, but the density of these features on the hillocks was considerably greater for samples polished with the coarser particle size.

An etching period of 30 s in concentrated HCl at room temperature was chosen for the preparation of devices as a compromise on the basis that shorter etching periods might not result in the removal of all of the polycrystalline work-damaged layer, whilst longer periods produce ledges and kink sites on hillocks. In fact the etching period of 30 s was split into two stages, the sample was first etched for 20 s after mechanical polishing. Next an indium ohmic contact was applied to the cadmium basal plane (usually) simply by pressing on a pellet of indium wire ($\sim$ 0.5 mm thick) and heating in an argon atmosphere at about 200^{o}C for 10 minutes to melt the indium. In this way an excellent ohmic contact was achieved. The second stage of the etching process lasting 10 s was carried out just before the heterojunction was formed.

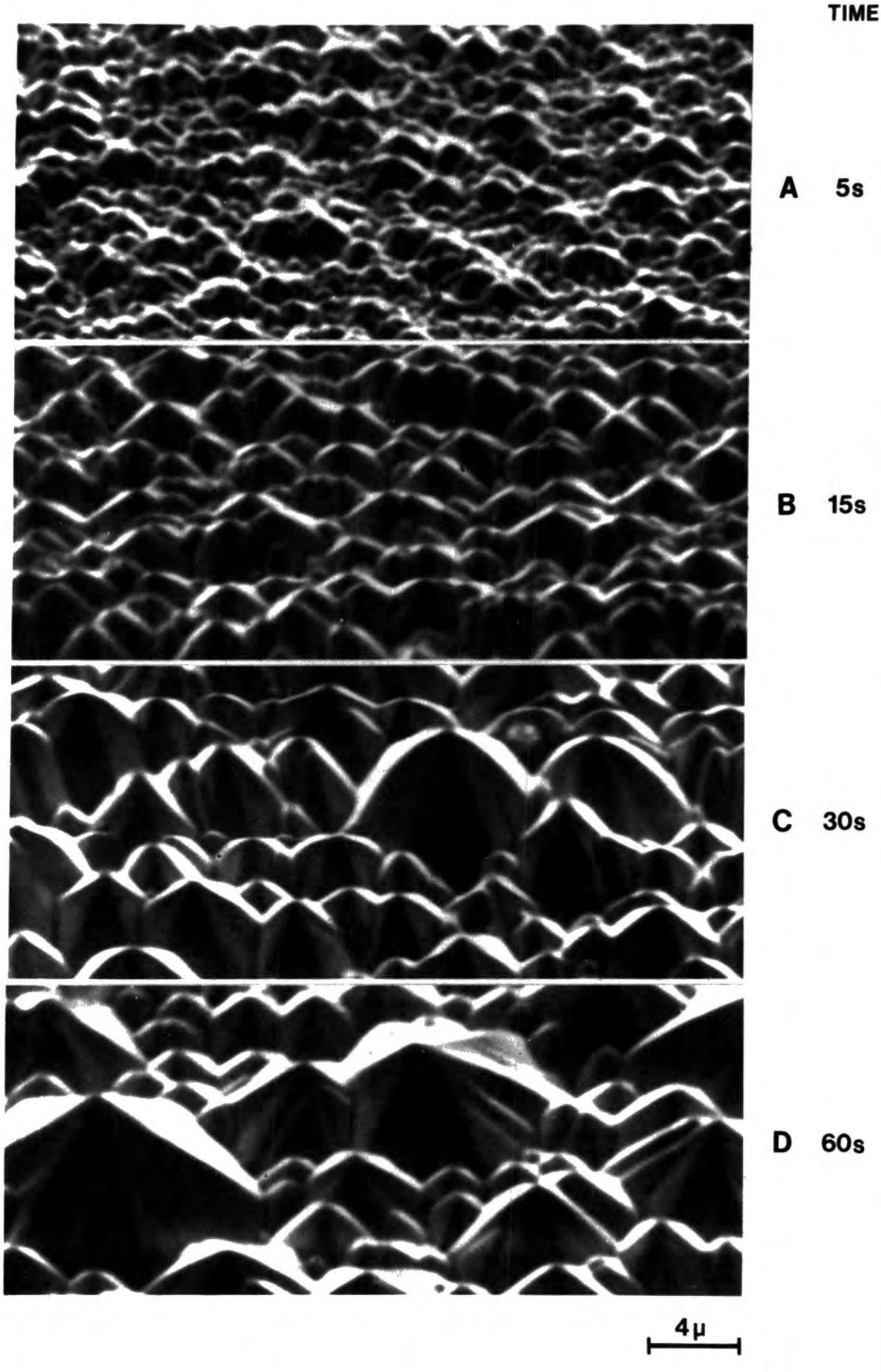


FIG.5·7(a) SECONDARY EMISSION MICROGRAPHS OF $(000\bar{1})$ CdS SURFACES ETCHED FOR DIFFERENT PERIODS (TYPE A POLISHED WITH 1 μ ALUMINA)

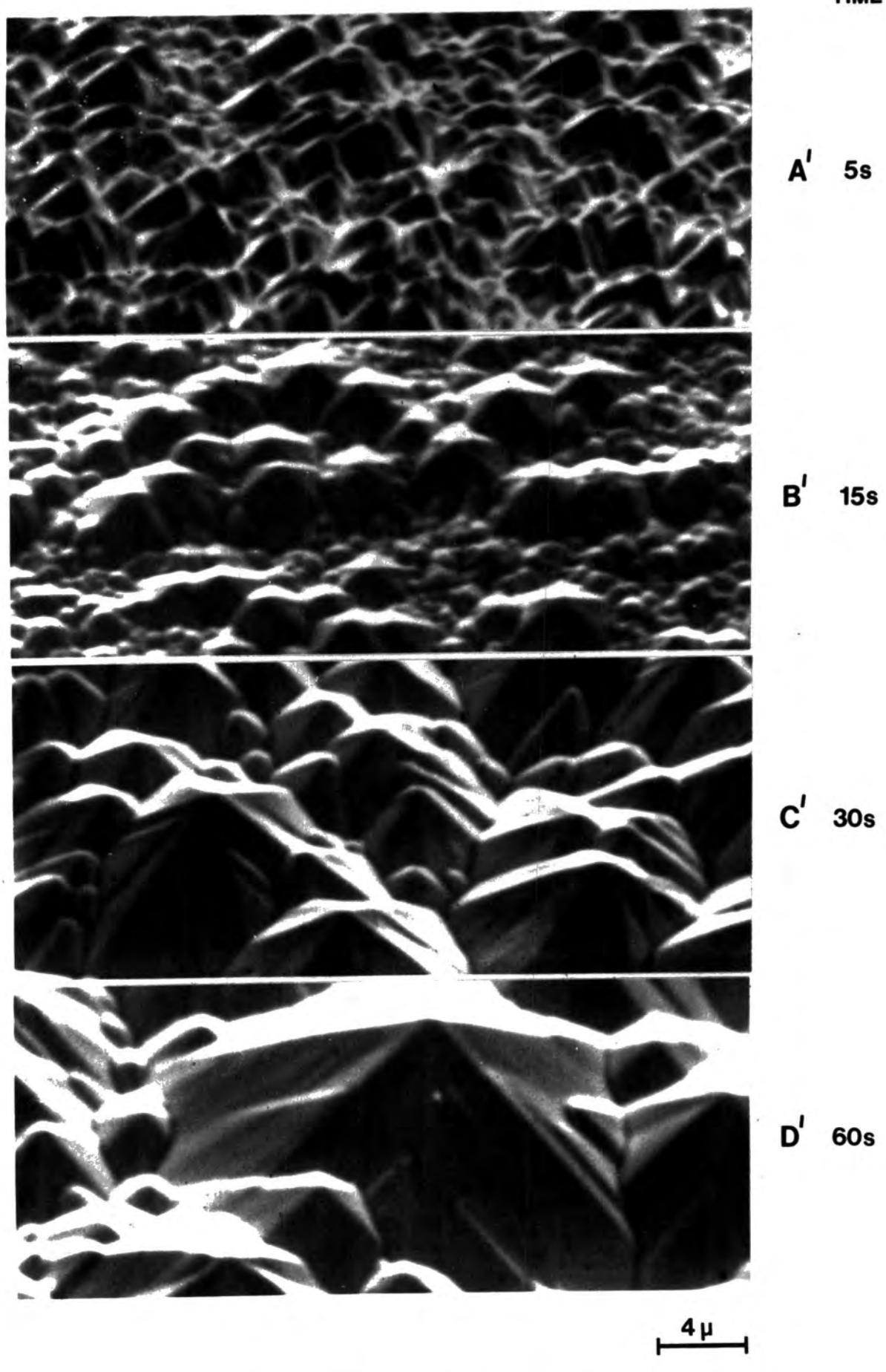


FIG. 5·7(b) SECONDARY EMISSION MICROGRAPHS OF $(000\bar{1})$ CdS SURFACES ETCHED FOR DIFFERENT PERIODS (TYPE A POLISHED WITH 5μ ALUMINA)

5.3 THE COPPER SULPHIDE LAYER

The primary role of the copper sulphide in CdS and (CdZn)S heterojunction cells is as a photon absorber. Thus its properties determine the light-generated current J_{LO}. Because of its importance the parameters involved in its preparation have been studied in detail. The first step was the improvement of the chemiplating technique by three significant modifications, which gave better control of the stoichiometry of the Cu_xS formed on the CdS. Following this, in an attempt to study the conversion process more closely, the rate of formation of Cu_xS using different techniques was examined. The phase of the Cu_xS produced under different preparative conditions and the phase changes resulting from further treatment were monitored using the RED technique. Moreover, the diffusion lengths of minority carriers in Cu_xS were measured (see Chapter 6) using the EBIC technique.

5.3.1 Formation of Cu_xS on CdS

The aim of this part of the work was to improve the chemiplating technique to gain control over the production of the chalcocite phase (Cu_2S) of copper sulphide. It is well established that chalcocite, Cu_2S is the only Cu_xS phase yielding high photovoltaic conversion efficiency when combined with CdS[4]. The basic method was essentially similar to that described by Caswell et al[5] with three important modifications. For the sake of completeness, the recipe for the chemiplating technique can be summarised as follows:

(1) 75 ml of deionized water was heated in a closed reaction vessel and then oxygen free nitrogen gas was bubbled through the liquid to remove any dissolved oxygen.

(2) 12 ml of concentrated HCl acid was added to the water, heating commenced and the nitrogen gas flow was continued.

(3) 7ml of hydrazine hydrate solution was added to the solution to produce a pH of 2 to 3 as measured by narrow range pH paper.

(4) 1 g of CuCl was added and the pH checked.

(5) After heating the solution to 95°C the pH was checked again and if necessary corrected by using a small amount of HCl or hydrazine hydrate.

(6) Chemiplating was carried out at about 95°C. To limit the growth of Cu_xS to the desired plane (usually the sulphur plane) all other faces of the dice were masked with acid resistant lacquer. The dice were then immersed in the solution for a time depending on the thickness of the layer required. After chemiplating, samples used initially to be washed in methanol and dried in the open laboratory. However, it was found that methanol dissolved some of the copper from the Cu_xS leaving a less copper rich phase behind. In order to produce the chalcocite phase of Cu_xS reproducibly, a number of modifications were made.

(i) Before the CuCl was added to the chemiplating bath, it was washed in a 10% solution of HCl to remove any Cu^{2+} (cupric) ions. It was then rinsed in acetone and dried in a vacuum.

(ii) The dice were etched in concentrated HCl for 10 s and then pre-heated in de-ionised water at 95°C before being immersed in the chemiplating solution.

(iii) After immersion for a required time in this solution, the dice were washed in de-ionised water and dried in a stream of dry nitrogen.

In fact when cells were made without these three modifications, it was very difficult to attain reproducibility of the phase of the Cu_xS. However, after these modifications were incorporated good reproducibility and uniformity of the chalcocite layer on the CdS was achieved.

The chemiplating process takes place in the solution by conversion of the CdS to Cu_2S. The displacement reaction

$$CdS + 2\ CuCl \rightleftharpoons Cu_2S + CdCl_2 \qquad (5.1)$$

occurs producing a layer of Cu_2S on the surface whilst cadmium chloride goes into the solution. This kind of conversion in which 1 Cd atom is exchanged

for 2 Cu^+ atoms leaving the sulphur sublattice intact is called topotaxy.

5.3.2 Thickness of the Cu_xS Layer and Rate of Growth

Thermodynamic considerations of the reaction (Eq. 5.1) indicate that it is highly favoured in the forward direction (for the standard free energy values see Ref (6)). In order to study the factors governing the rate of conversion of single crystal CdS to Cu_2S, the thicknesses of the grown layers have been measured using two different methods.

(1) The first method involved chemical dissolution of the Cu_2S layer in 1 ml of fuming HNO_3 acid and dilution of this solution with 4 ml of de-ionised water followed by a spectrophometric analysis of this solution.

The accuracy of the assessment of the quantity of Cu in solution was quite high with this technique. Hence thicknesses were calculated as a function of plating time using the measured copper content and assuming the copper sulphide layer to be a slab (the nominal area used was 0.16 cm^2). The results are tabulated in Table 5.1.

TABLE 5.1: Thickness of Cu_2S layer on etched $(000\bar{1})$ plane of the CdS as a function of the chemiplating period determined by the chemical dissolution method.

Dipping Time (seconds)	Cu measured (ppm)	Calculated Thickness (μm)
10	4.4	0.95
30	8.6	4.70
60	34.4	7.40
120	69.2	14.50
300	157.2	34.00

The major error in this method is associated with the very complex

topographical area of the Cu_xS surface and the $CdS-Cu_2S$ interface. Indeed this error is very large for short period plating and decreases as the immersion period is extended. For instance, the actual area of Cu_2S is thought to be four times larger than the nominal area in a 10 s dipped cell. Thus the actual thickness of the Cu_2S layer is probably about $\sim$ 0.25 μm.

(2) The second method used to determine the thickness of the Cu_2S layer was to examine a cleaved cross-section perpendicular to the junction in the SEM using the SE mode. Fig 5.8 illustrates some typical cross-sections for Cu_2S layers grown on the sulphur plane of etched CdS for plating periods up to 1 hour. The average thickness values measured are given in Table 5.2.

TABLE 5.2 : Thickness of Cu_2S layers on the sulphur plane of etched CdS as a function of the chemiplating period. Thickness measured from cleaved cross-section of junction using the SEM.

Chemiplating Period	Average Thickness of Cu_xS layer μm
20 seconds	0.98
30 "	1.97
40 "	3.11
60 "	5.42
80 "	7.00
120 "	9.98
180 "	13.85
240 "	16.25
300 "	18.90
1 hour	85.00

The variation of thickness with plating time describes an approximately parabolic shape as shown by the curve in Fig 5.9 with the open circles. In the same figure the triangles demonstrates that the thickness

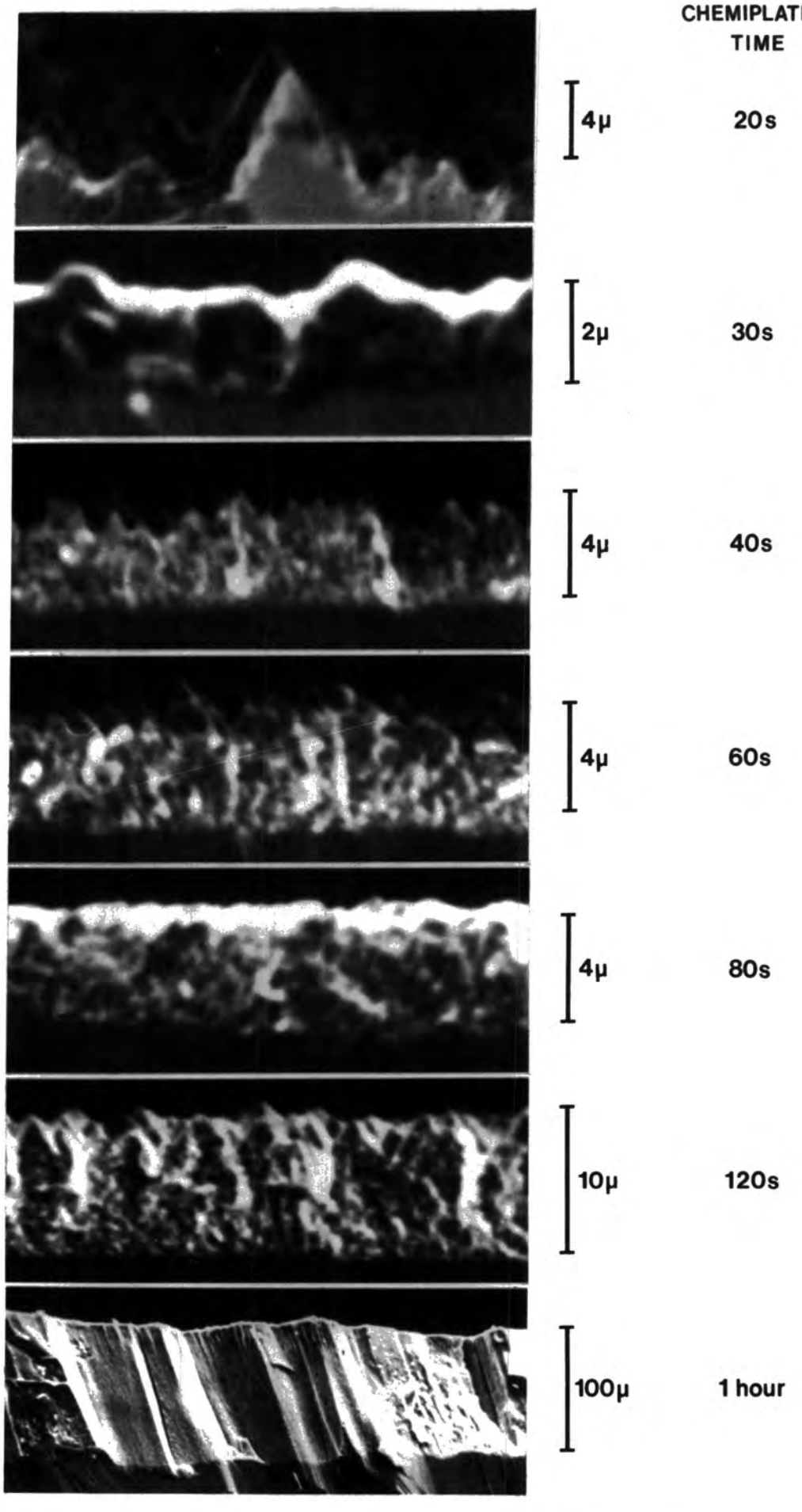


FIG. 5·8 SECONDARY EMISSION MICROGRAPHS OF CROSS-SECTION THROUGH CdS / Cu_2S JUNCTION (ETCHED FOR 30 s) CHEMIPLATED FOR DIFFERENT PERIODS

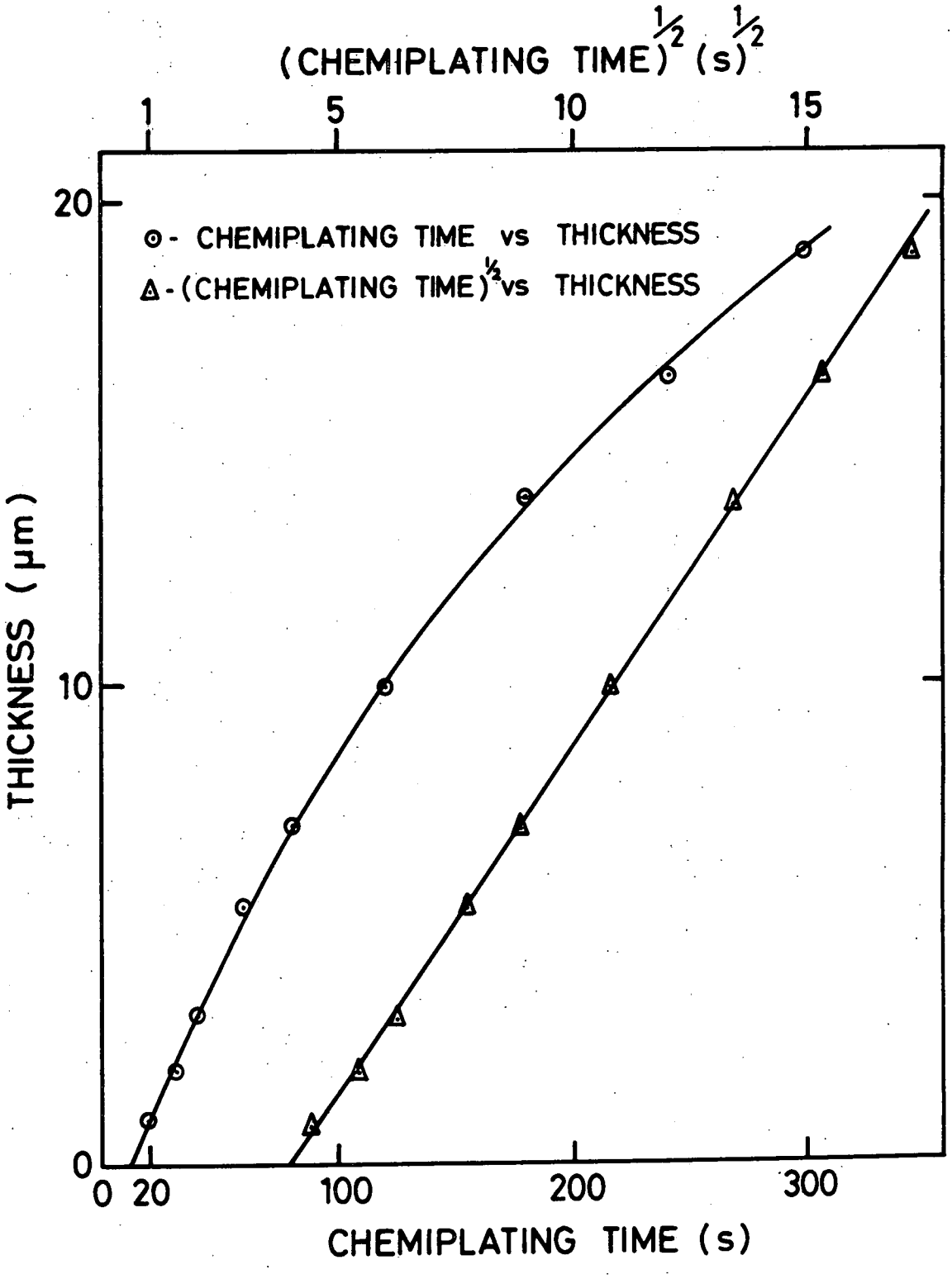


FIG. 5·9 THE INCREASE IN THICKNESS OF THE CONVERTED LAYER OF COPPER SULPHIDE AS A FUNCTION OF CHEMIPLATING TIME

of the Cu_2S layer is proportional to the square root of the time for periods from 20 s up to 300 s. However, this straight line does not go through the origin indicating that the initial conversion process cannot be described by the same parabolic law.

Unfortunately, with the technique used it was not possible to meaure the thickness of the converted layer for plating periods shorter than 20 s.

With the Cu_2S layer grown on mechanically polished surfaces and on the faces at different crystal orientations, the rate of growth was found to be strongly dependent on the surface preparation and crystal orientation. This is demonstrated by the SE micrographs shown in Fig 5.10 where the thicknesses are 5.42 μm, 2.67μm, 2.20 μm and 1.05 μm on an etched $(000\bar{1})$ surface and (0001) surface on a polished surface and on a randomly oriented etched surface.

5.3.3 The Phases of Copper Sulphides on CdS

The phases of Cu_xS layers grown on the CdS single crystals have been studied using reflection electron diffraction (RED). The fundamentals of this technique are described in chapter 4. In fact RED has been employed by several workers to investigate the phases of the Cu_xS systems[7,8,9].

The composition region of interest for solar cells extends from chalcocite ($Cu_{2O}S$) to the hexagonal phase ($Cu_{1.8-1.96}S$). Thus phases with composition outside this range were not investigated. Furthermore, the layers were usually formed on the sulphur faces $(000\bar{1})$ of the CdS, so that the junction approximated to cells prepared on CdS thin films. As is well known the crystallites of an evaporated CdS film are columnar, with the +C axes approximately perpendicular to the substrate[10]. In addition to this , diffraction patterns taken from the Cu_xS layers grown on the cadmium faces (0001) of CdS were less sharp than those from Cu_xS on the sulphur faces, because the smoother surface of the Cd plane gave rise to streaks through

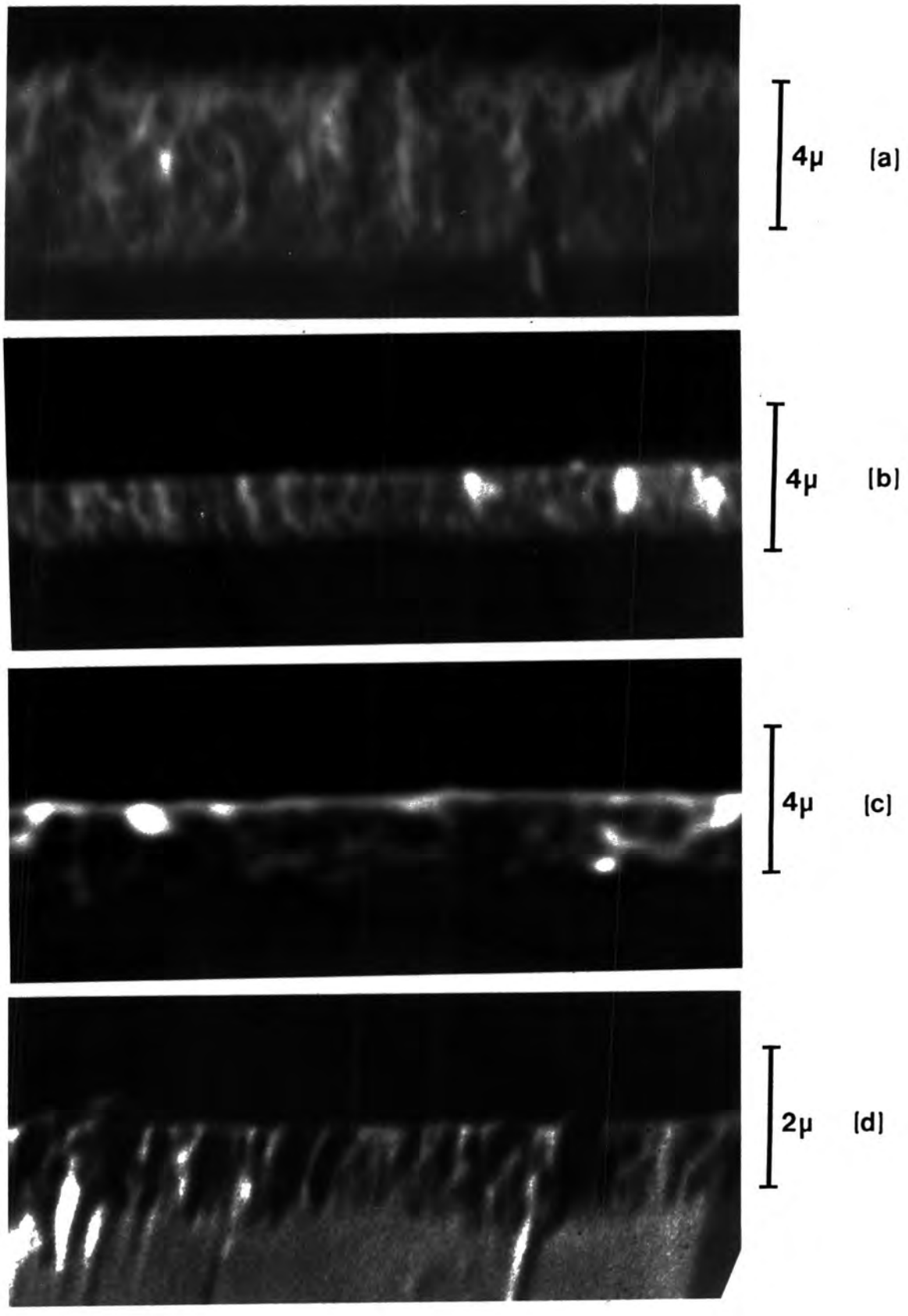
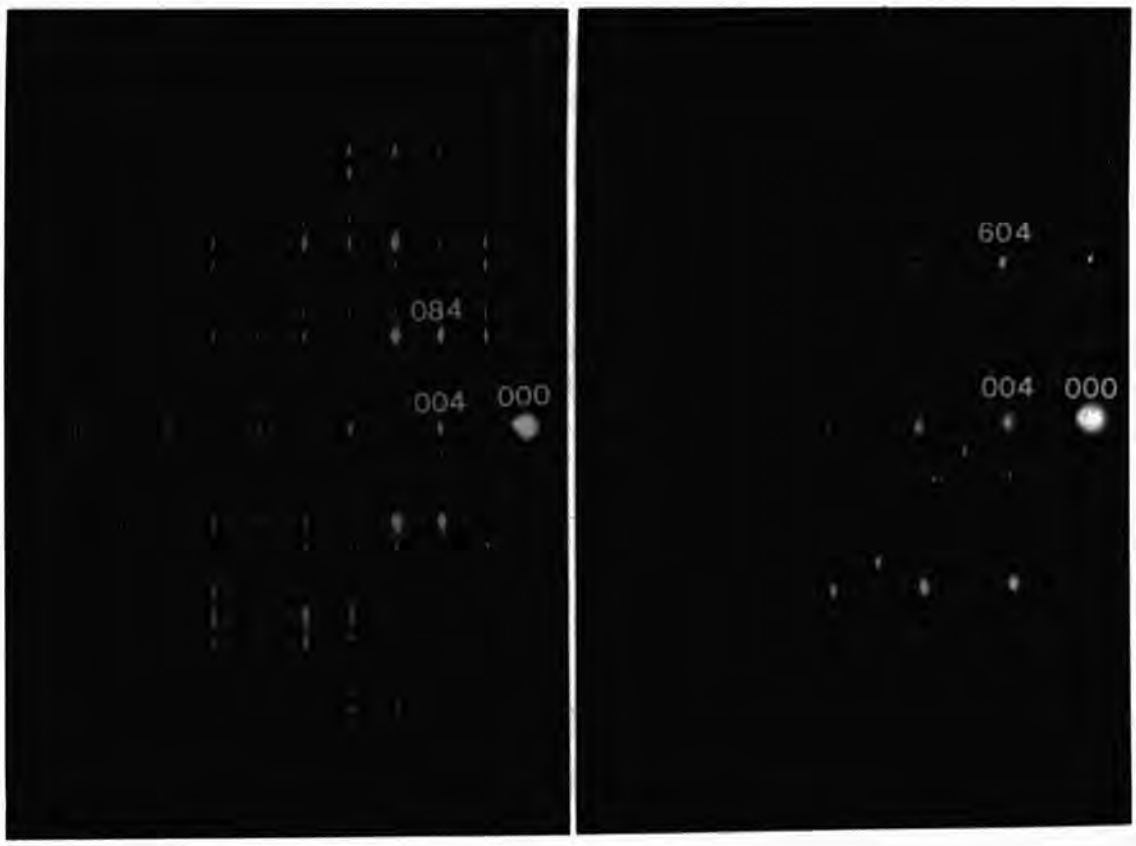


FIG. 5·10 SECONDARY EMISSION MICROGRAPHS OF A CROSS-SECTION THROUGH A CdS/Cu_2S JUNCTION CHEMIPLATED FOR 1 MIN. (a) ON ETCHED ($000\bar{1}$) PLANE, (b) ON ETCHED (0001) PLANE, (c) ON POLISHED SURFACE, (d) ON ETCHED NON-ORIENTATED CdS.

the diffraction spots.

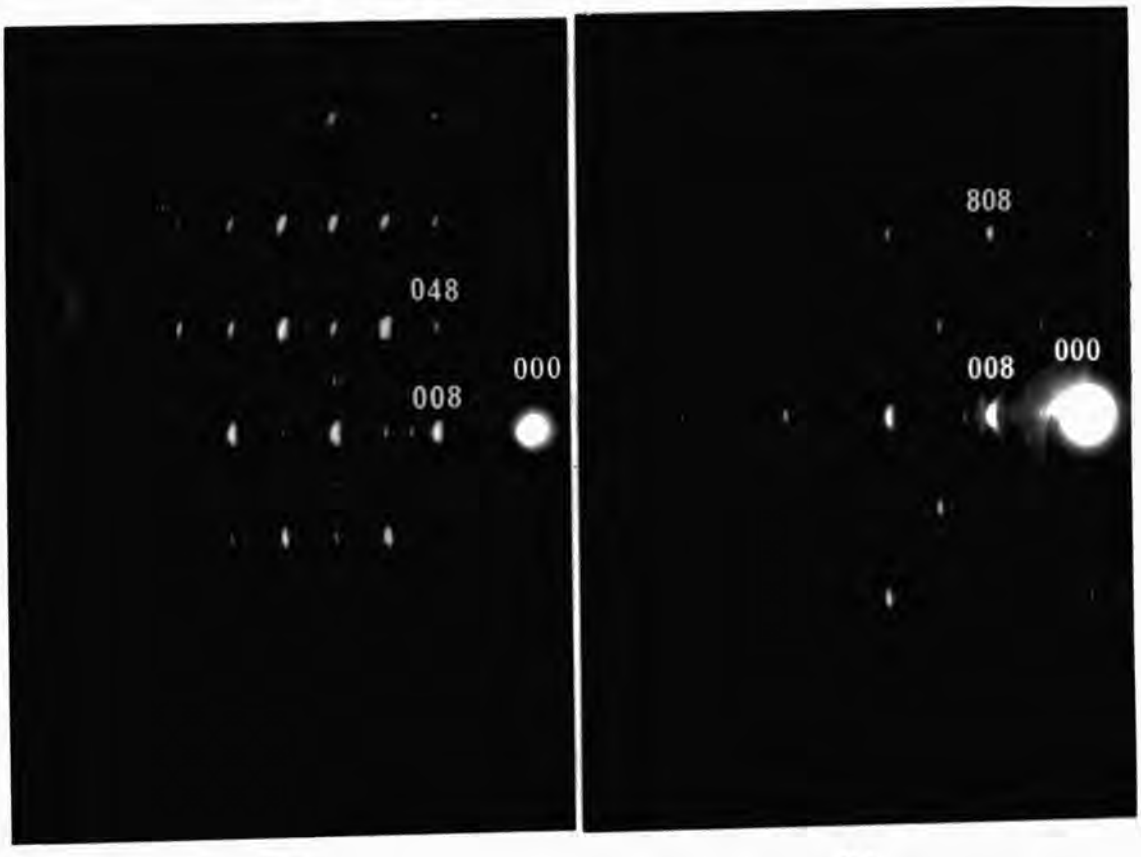
Throughout this work the phase of the Cu_xS layer on every cell has been investigated at various stages : (1) immediately after chemiplating, (2) after deposition of the top gold contact, (3) after the administration of a post barrier air-bake (4) at various intervals while the samples were left in the open atmosphere for periods of up to one year.

As electrons only penetrate the surface of a material to a depth of the order of tens of Angstroms, the information provided by the RED technique is limited to thin layers. The observed RED patterns were associated with a particular phase or mixture of phases by comparing them directly with those reported by Russell and Woods[9]. RED patterns corresponding to two low index directions which lay in the basal plane of the CdS substrates, and which were related by a 30° rotation about the c-axis of CdS were investigated. When the electron beam is incident parallel to a $\langle 10\bar{1}0\rangle$ direction (or a-axis), the orientation is referred to as a "normal" orientation, and when the beam is parallel to a $\langle 11\bar{2}0\rangle$ direction the orientation is described as a "30° position". The RED patterns obtained at the normal orientation and after a 30° rotation for one of the devices which was chemiplated using a modified technique at $95^{\circ}C$ for 10 s are shown in Figs 5.11(a) and 5.11(b) respectively. Following the paper by Russell and Woods[9] these patterns are identified as the chalcocite phase of copper sulphide corresponding to the [100] and [010] zone axes respectively. Because the [100] and the [010] zone axes are orthogonal the pattern shown in Fig 5.11(b) is expected after a 90° rotation of the sample about the c-axis from the position in which the pattern in Fig 5.11(a) was obtained. In fact a 30° rotation around the c-axis resulted in the pattern in Fig 5.11(b). Nevertheless a 90° rotation gave rise to the same pattern. Thus, even though the spot pattern indicates a single crystal structure, there must be different sets of grains which give rise to the "30° position" pattern. This conflict may be explained by the crystallographic relation between the hexagonal CdS



(a) (b)

Fig 5.11: RED patterns of chalcocite (a) "normal" orientation (b) after a rotation of 30° about the c-axis.



(a) (b)

Fig 5.12: RED patterns of djurleite (a) "normal" orientation (b) after a rotation of 30° about the c-axis.

and the orthorhombic Cu_2S. It is well known that the CdS c-axis and chalcocite a-axis coincide[11], and as shown in Chapter 2 (Fig 2.1(a)) the hexagonal CdS lattice has three equivalent but geometrically different a-axes. Hence there are three possible orientations with the common c-axis for the orthorhombic chalcocite to come into existence on the sulphur sublattice of the hexagonal CdS topotaxially. Fig 5.13(a) illustrates these three possible orientations of the unit cell of chalcocite relative to the CdS substrate (labelled L, M, R). Such grains might be expected to give rise to more complex RED patterns. However, the reasons for the observed single crystal spot patterns and the appearance of the [010] zone axis reflections after a 30° rotation can be understood in the light of the preceding discussion, see Russell and Woods[9]. When the beam is incident along the a-axis [100] of the unit cell M it is also incident along $\langle 430 \rangle$ directions in each of the unit cells labelled L and R (i.e. the other possible two grains of chalcocite). Russell and Woods[9] have shown that reflections from the different orientations are coincident within the limits of experimental error. In a similar way an electron beam incident along the b-axis, [010], directions of the unit cell M, is simultaneously incident along $\langle 410 \rangle$ directions in the unit cells L and R. Again, it can be shown[9] that the reflections from the two different zone axes are coincident within the limits of the technique. Thus even though the patterns in Figs 5.11(a) and 5.11(b) arise from three different groups of grains of chalcocite, they appear as a single crystal spot pattern. Further, the relatively more intense reflections, which form the sub-lattice of patterns in Fig 5.11(a) and 5.11(b) can be attributed to these coincident diffracted beams from grains in each of the possible orientations.

Evidently then the appearance of a pattern expected from the [010] zone axis, as the sample is just rotated through 30°, instead of 90°, can be attributed to the beam incident along the b-axis of the unit cell L or R

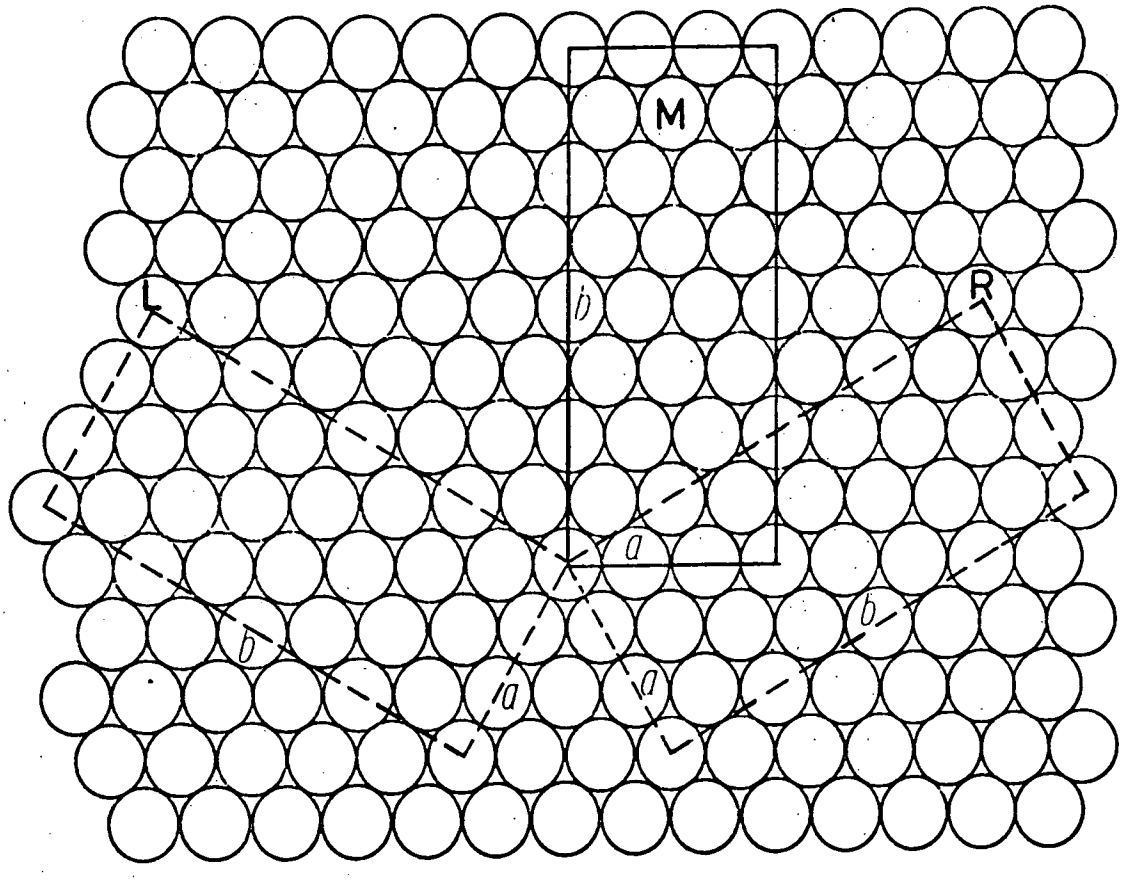


FIG.5·13(a) THE THREE POSSIBLE ORIENTATIONS OF THE ORTHORHOMBIC UNIT CELL OF CHALCOCITE IN THE BASAL PLANE OF CdS.

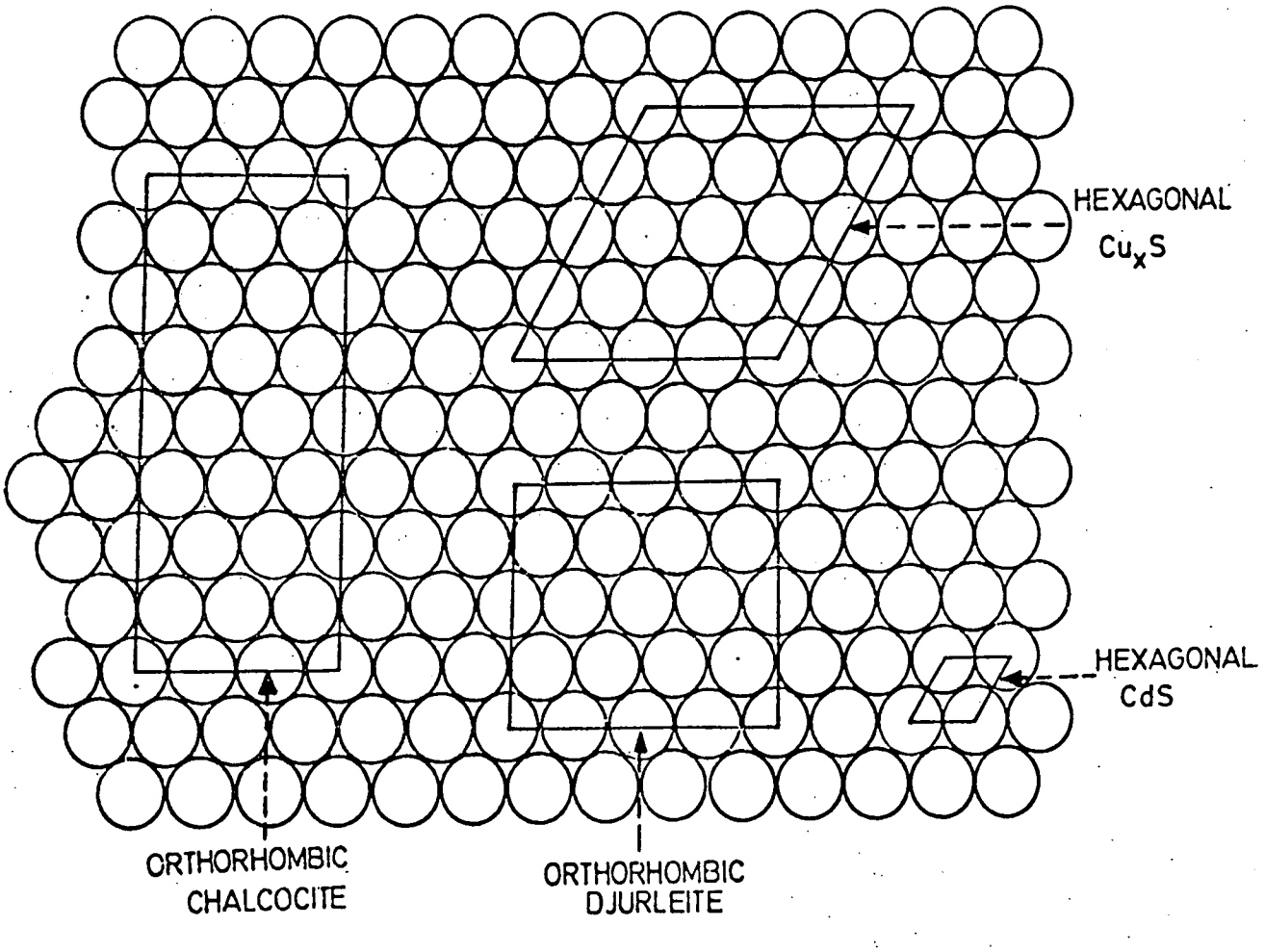


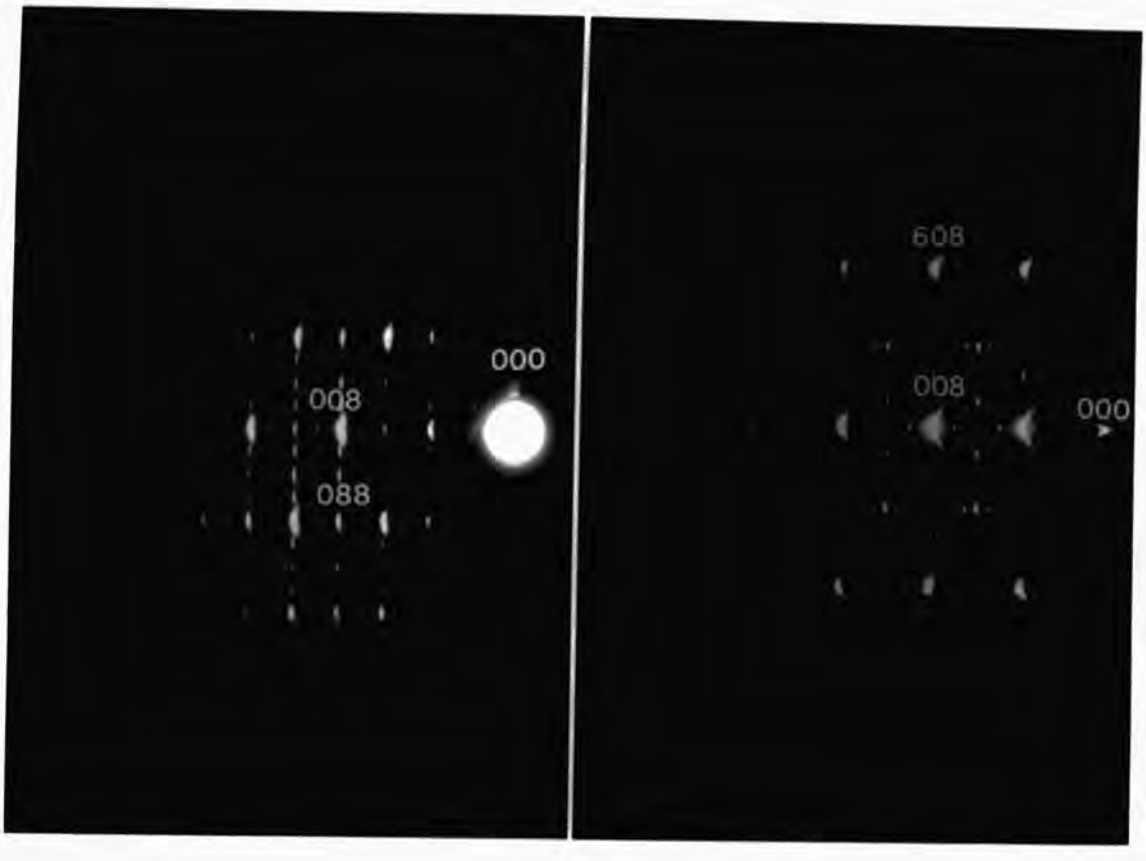
FIG.5·13(b) IDEALISED UNIT CELLS FOR THREE PHASES OF Cu_xS (FOR $x \triangleq 2$) SHOWING RELATIVE SIZE AND ORIENTATION IN THE BASAL PLANE OF HEXAGONAL CdS.

depending upon the direction of rotation about the c-axis. In fact, a 90^{o} rotation of the sample from the normal position gave rise to the same pattern. Thus the positions reached by a 30^{o} or a 90^{o} rotation from a normal position are identical.

By following the same method, the RED patterns given in Fig 5.12(a) and 5.12(b) were found to correspond to reflections from the [100] and the [010] zone axes of the djurleite phase of copper sulphide respectively. These patterns were obtained from the sample chemiplated at a lower temperature ($\sim 85^{o}$). A similar analysis can be carried out for the crystallographic relationship between orthorhombic djurleite and hexagonal CdS since the principle involved is the same for each phase of copper sulphide. In addition, in comparing the unit cells of chalcocite and djurleite (Fig 5.13(b)), the spots at double distance apart in the RED patterns in Fig 5.12(a) and 5.12(b) can easily be explained using reciprocal lattice vectors.

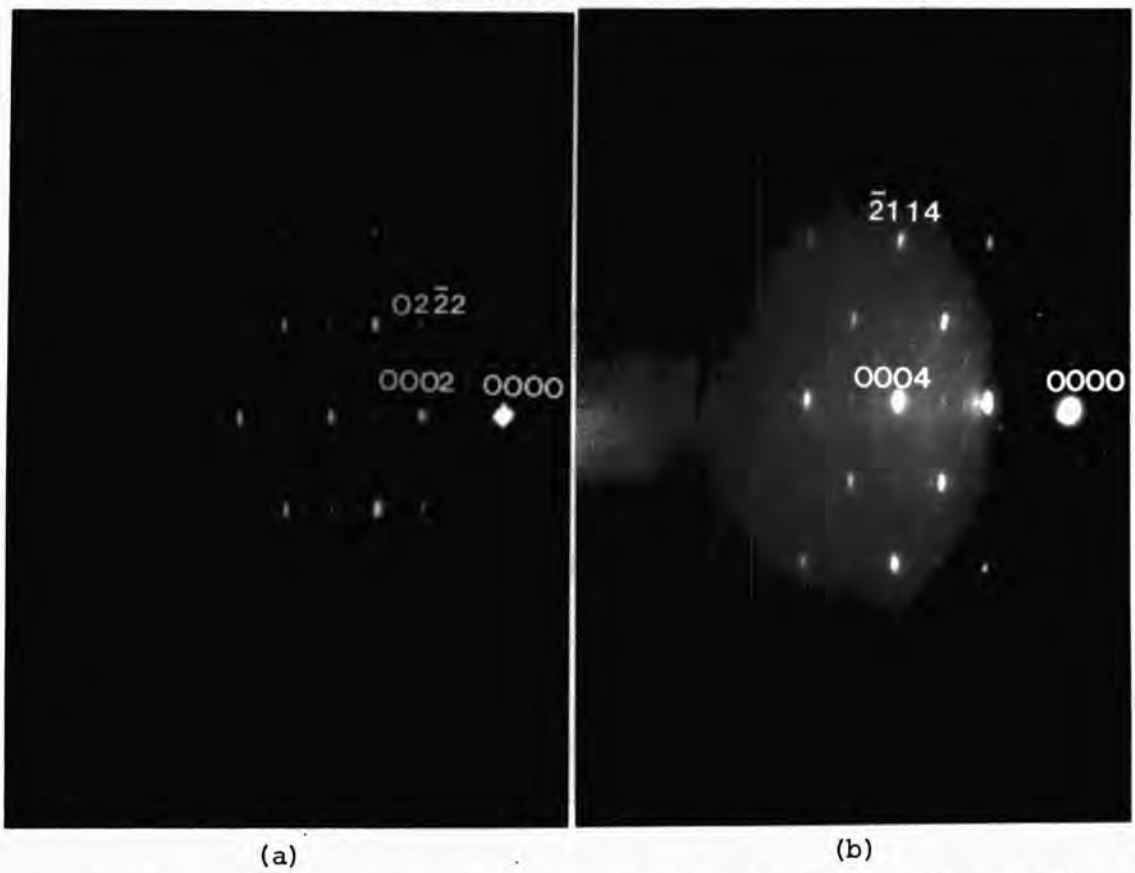
Although no evidence of djurleite was detected in the RED patterns from the Cu_2S layers obtained using the improved chemiplating technique described earlier a small amount of djurleite was always present in these layers. Evidence for this comes from measurement of the photoresponse described in section. Evidently any small deviation in the plating parameters results in a large change in the compsotion of the Cu_xS layer. Before the chemiplating technique was modified, the RED patterns quite often indicated a mixture of the chalcocite and djurleite phases. Figs 5.14(a) and 5.14(b) show the RED patterns from a mixture of chalcocite and djurleite at normal orientation and after 30^{o} rotation.

The phase produced by chemiplating a CdS single crystal CdS at about $70^{o}C$ in the modified plating bath yielded the RED patterns shown in Figs 5.15(a) and 5.15(b). By analysing these in the same way as before it has been established that they can be attributed to a normal and 30^{o} position of hexagonal grains of Cu_xS ($1.96 \leqslant x \leqslant 1.8$)[11]. In fact a close analysis of the djurleite RED patterns revealed that they contained some hexagonal Cu_xS .



(a) (b)

Fig 5.14 : RED pattern of chalcocite-djurleite mixture
(a) "normal" orientation (b) after a rotation of 30° about the c-axis.



(a) (b)

Fig 5.15 : RED pattern of hexagonal phase of Cu_xS ($1.96<x<1.80$)
(a) "normal" orientation (b) after a rotation of 30° about the c-axis.

Because the djurleite and the hexagonal phases have the same a-axis in the same sulphur sublattice, it is difficult to detect a small quantity of the hexagonal phase in the presence of the predominant djurleite phase and vice versa. Because CdS and most of the copper sulphide phases have a virtually identical sulphur network[11] and the cadmium or copper atoms take on various types of ordering within this framework one may easily be converted to another.

5.4 PERFORMANCE OF AS-MADE CdS/Cu_2S HETEROJUNCTIONS AS SOLAR CELLS

After the identification of the phase of Cu_xS on the single crystal CdS, electrical contact was made to the copper sulphide layer with an evaporated gold electrode 1 mm in diameter. Current-voltage characteristics were then recorded for all devices both in the dark and under 100 mW/cm^2 (AM1) incident illumination. These provided an insight into the basic electrical behaviour of a cell and also into the relationship between the performance of a cell and its preparation.

As-plated CdS/Cu_2S heterojunctions formed on the sulphur planes of optimum resistivity (0.5 - 5.0 Ω cm) undoped CdS crystals can be divided into two groups as far as their dark diode characteristics and photovoltaic performance are concerned. A junction formed on a sulphur plane with etch features similar to those shown in Fig 5.5 (type A surfaces with an array of smooth facetted hillocks) carrying a layer of chalcocite produced by the optimised plating process exhibited the following features : (i) excellent rectification (ii) small leakage current and high breakdown voltage (≥5V) in reverse bias and (iii) high performance as a solar cell with efficiency η(AM1) of up to 5.3% and fill factor of 0.69. An additional important property of these cells was that no significant deterioration occurred during storage in the laboratory atmosphere for three months. Typical current-voltage characteristics of such a type A cell measured in the dark and under AM1 illumination are illustrated in Fig 5.16.

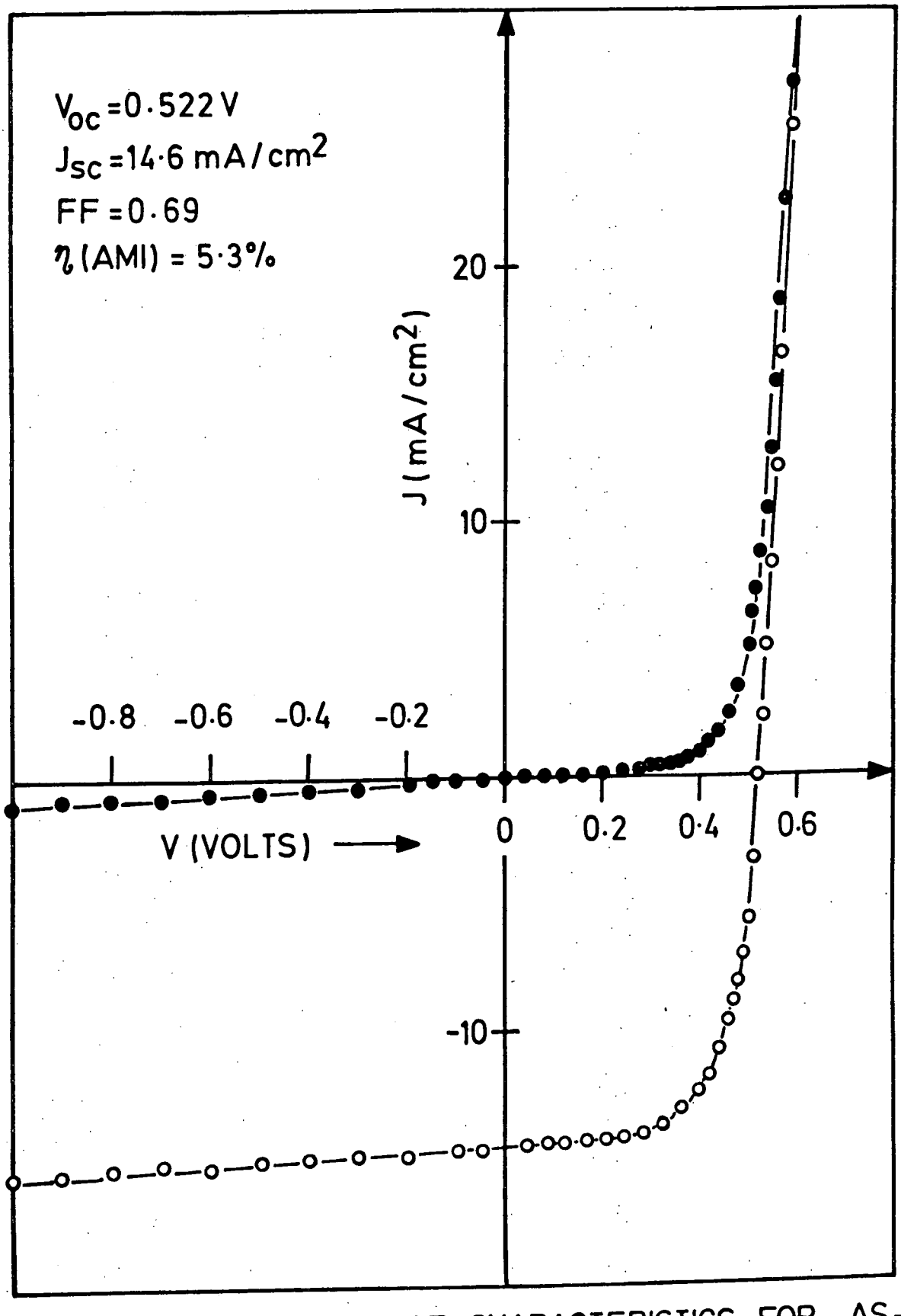


FIG. 5·16. CURRENT – VOLTAGE CHARACTERISTICS FOR AS-MADE TYPE A CELL MEASURED IN THE DARK AND UNDER 100 mW cm^{-2} ILLUMINATION.

In contrast, current-voltage analysis of devices formed on type B surfaces (Fig 5.6, with numerous kink sites and ledges on the sides of the hillocks) using the same plating procedure revealed the following features : (i) poor diode behaviour in the dark with very high leakage current, (ii) poor photovoltaic behaviour with an as-made efficiency, η(AM1) of about 0.3% and fill factors of 0.25. Representative current-voltage characteristics for as-plated type B cells are shown in Fig 5.17. The rectification and photovoltaic performance of type B devices was better for cells formed on faces with fewer ledges and kink sites. Nevertheless a device made on a type B surface could never be made to achieve the excellent rectifying and high photovoltaic performance of cells made on type A surfaces.

Another interesting feature is that the current-voltage characteristics of as-plated type A and B devices measured in the dark and under AM1 illumination converged towards each other at high forward bias and did not cross over. With each type of cell the reverse voltage curve under illumination can approximately be described as the displacement downwards of the dark reverse curves by an amount determined by J_{SC}.

In order to assess the importance of etching the surface of CdS before preparing the Cu_xS layer a number of junctions were formed by growing the Cu_xS directly onto as polished surfaces. The resultant cells exhibited reasonable dark-diode characteristics (Fig 5.18), but under illumination light induced reverse breakdown occurred at about -1.0V. Further, in forward bias the light and dark characteristics crossed over even in the as-made condition. Both the light induced reverse bias breakdown and the forward bias cross-over became less significant as the chemiplating period was extended. The photovoltaic properties of the devices made on polished surfaces were far inferior to those of devices made on etched surfaces.

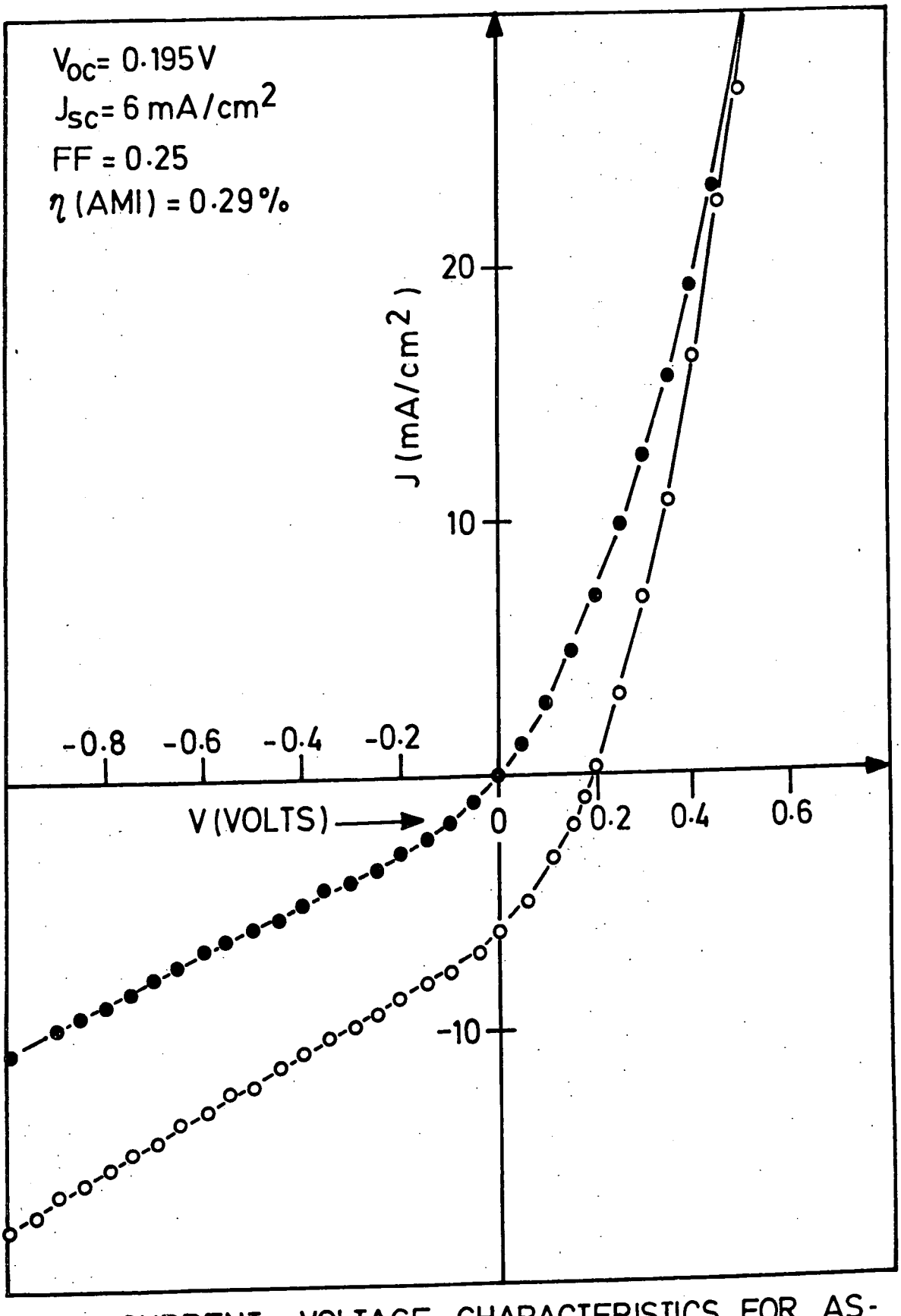


FIG.5·17. CURRENT—VOLTAGE CHARACTERISTICS FOR AS-MADE TYPE B CELL MEASURED IN THE DARK AND UNDER 100 mW cm^{-2} ILLUMINATION.

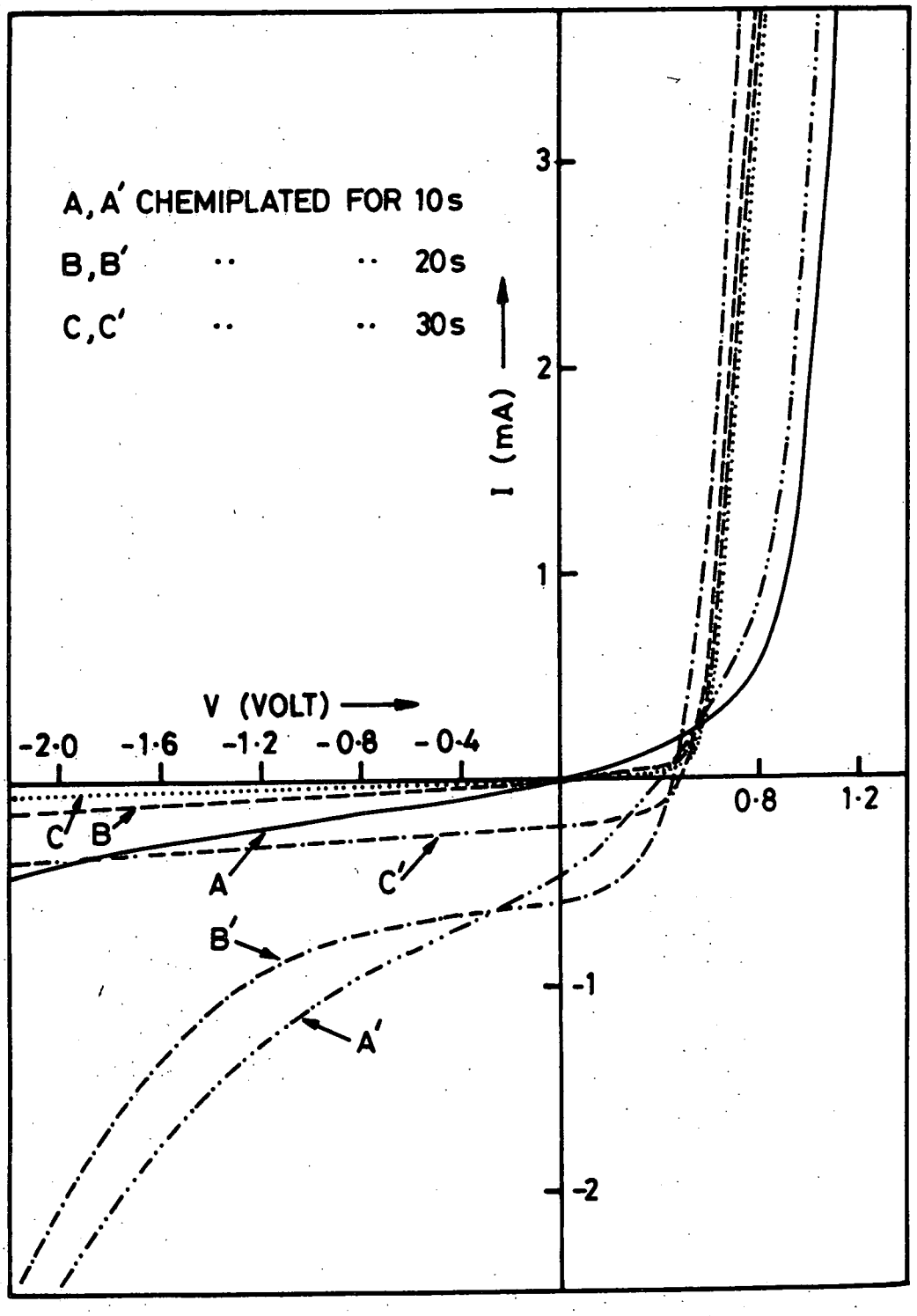


FIG. 5·18 CURRENT-VOLTAGE CHARACTERISTICS FOR AS-MADE CdS/Cu_2S CELLS FORMED ON POLISHED SURFACE, FOR DIFFERENT CHEMIPLATING TIME, MEASURED IN THE DARK (A,B,C) AND UNDER AMI ILLUMINATION (A',B',C')

5.5 SPECTRAL RESPONSE OF AS-MADE DEVICES

In an attempt to determine whether there was a correlation between the spectral response and the overall performance of a device under AM1 illumination, the spectral dependence of V_{OC} and I_{SC} of almost every device made was measured. The second purpose of these measurements was to provide information about the fundamental device mechanisms and to relate the RED observation on the Cu_xS layers to the spectral response. The response of cells was recorded over a wavelength range from 0.4 to 2.0 μm.

The spectral distribution of V_{OC} and I_{SC} at room temperature (22°C) for a device prepared using the improved plating technique, is shown in Fig 5.19. The layer of copper sulphide was identified as predominantly chalcocite from RED examination. The important features of these spectral response curves are : (1) the shapes of the V_{OC} and I_{SC} responses are very similar; (2) the magnitude of V_{OC} at the maximum point in the spectral response was five times less than that measured under AM1 (100 mW cm^{-2}) illumination, whereas the difference was two orders of magnitude for I_{SC}; (3) both V_{OC} and I_{SC} curves showed the maximum response at about 0.96 μm with a broad shoulder in the vicinity of a 0.70 μm, while the peak at 0.52 μm was only just apparent at the same sensitivity. However, when the sensitivity was increased fivefold the existence of the peak at 0.52 μm was more evident. The curves in Fig 5.19 were obtained from a device which had good rectification characteristics and high photovoltaic efficiency (type A device). The spectral distribution of V_{OC} and I_{SC} for as-prepared type B cells with predominantly chalcocite layers were very similar to those observed for type A cells with chalcocite layers. However, the magnitudes of the maximum responses were nearly three times less than those for type A cells. In Fig 5.19 the two major peaks at wavelengths of 0.96 μm and 0.70 μm correspond respectively to the absorption of light across the indirect band gap of chalcocite (1.2 eV)[12] and across the direct band gap of djurleite (1.8 eV)[13]. The small peak at 0.52 μm represents the photovoltaic

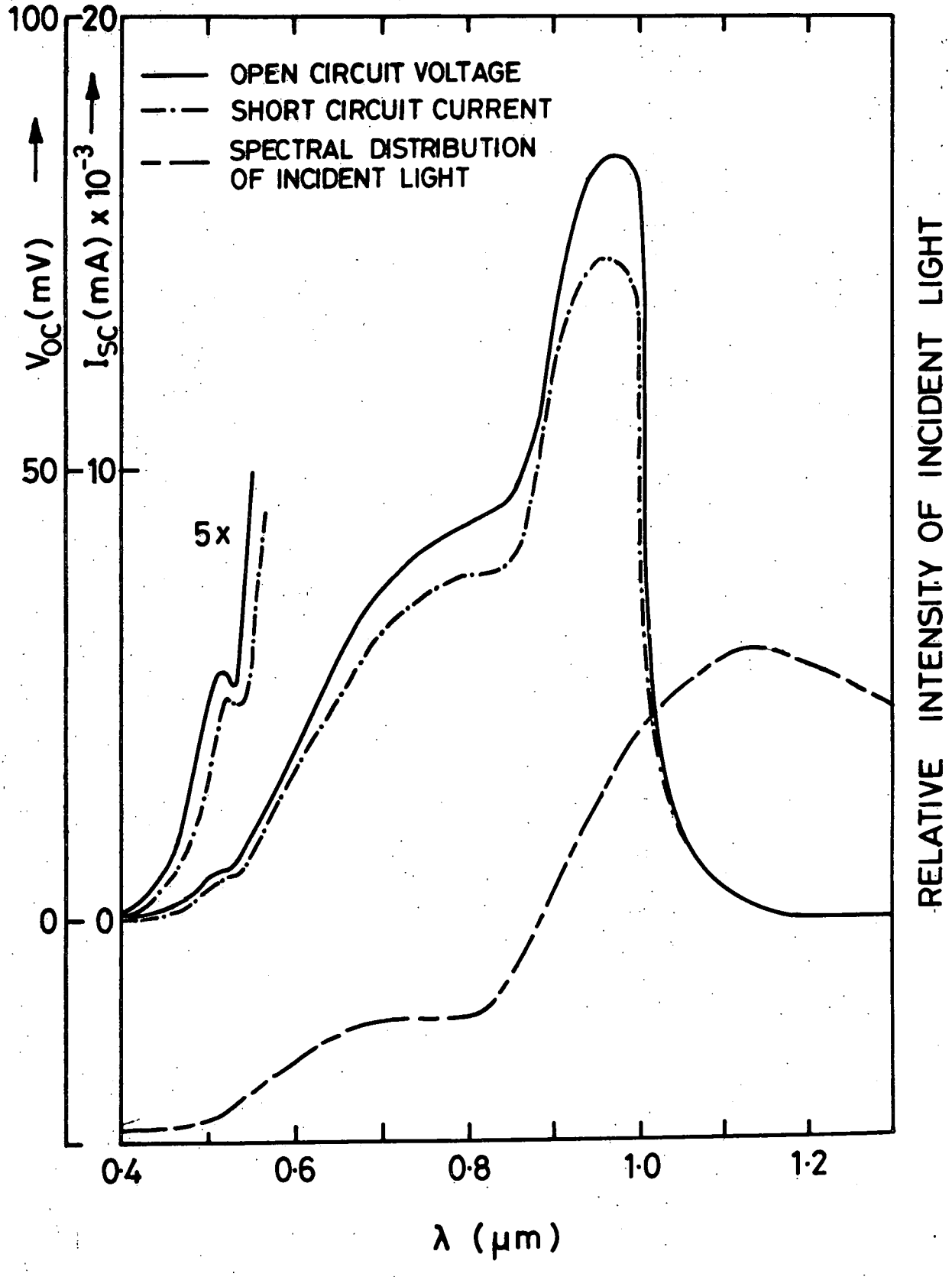


FIG. 5·19. SPECTRAL RESPONSE OF V_{OC} AND I_{SC} AT ROOM TEMPERATURE FOR AS-MADE, TYPE A, CdS/Cu_2S CELL

response accompanying light absorption in the CdS.

As indicated earlier before the chemiplating and drying process were improved the reproducibility of the chalcocite phase was not high. RED examination has shown that the layers produced were quite often mixtures of chalcocite and djurleite in various ratios. The relative spectral response of V_{OC} for as-made cells on which Cu_xS layers have been identified as (a) chalcocite (continuous line), (b) chalcocite dominant (dashed line) and (c) djurleite dominant (dashed-dotted line) mixtures of chalcocite and djurleite are shown in Fig 5.20. In this diagram the change in the ratio between the two longer wavelength responses gives further evidence for the association of the peaks at 0.96 μm and 0.7 μm with absorption in the chalcocite and djurleite respectively. Incidentally, the response at 0.52 increased as the peak at 0.69 μm (djurleite) increased.

In order to demonstrate the correlation between the phase of Cu_xS and the spectral response of a cell more clearly, the spectral distribution of V_{OC} and I_{SC} for devices formed by chemiplating at 85°C and 70°C are shown in Figs 5.21 and 5.22 respecitvely. As described earlier (5.3.3) RED examination showed that the phase produced at 85°C was wholly djurleite and that at 70°C was hexagonal Cu_xS ($1.96<x<1.8$). It is well established that a lower plating temperature leads to a thinner layer of copper sulphide overall[14]. Thus, as the plating temperature was reduced to 80°C and 70°C its duration had to extend to 15 s and 20 s. respectively in order to ensure that the thickness of the copper sulphide was comparable to that produced at the customary chemiplating temperature (95°C). With a cell formed by chemiplating at 85°C(Fig 5.21) two large peaks were apparent at 0.69 and 0.52 μm. There was a small shoulder near 0.96 μm. The large response at the band gap of CdS indicates that a considerable proportion of the light passed through the Cu_xS layer to be absorbed in the underlying CdS.

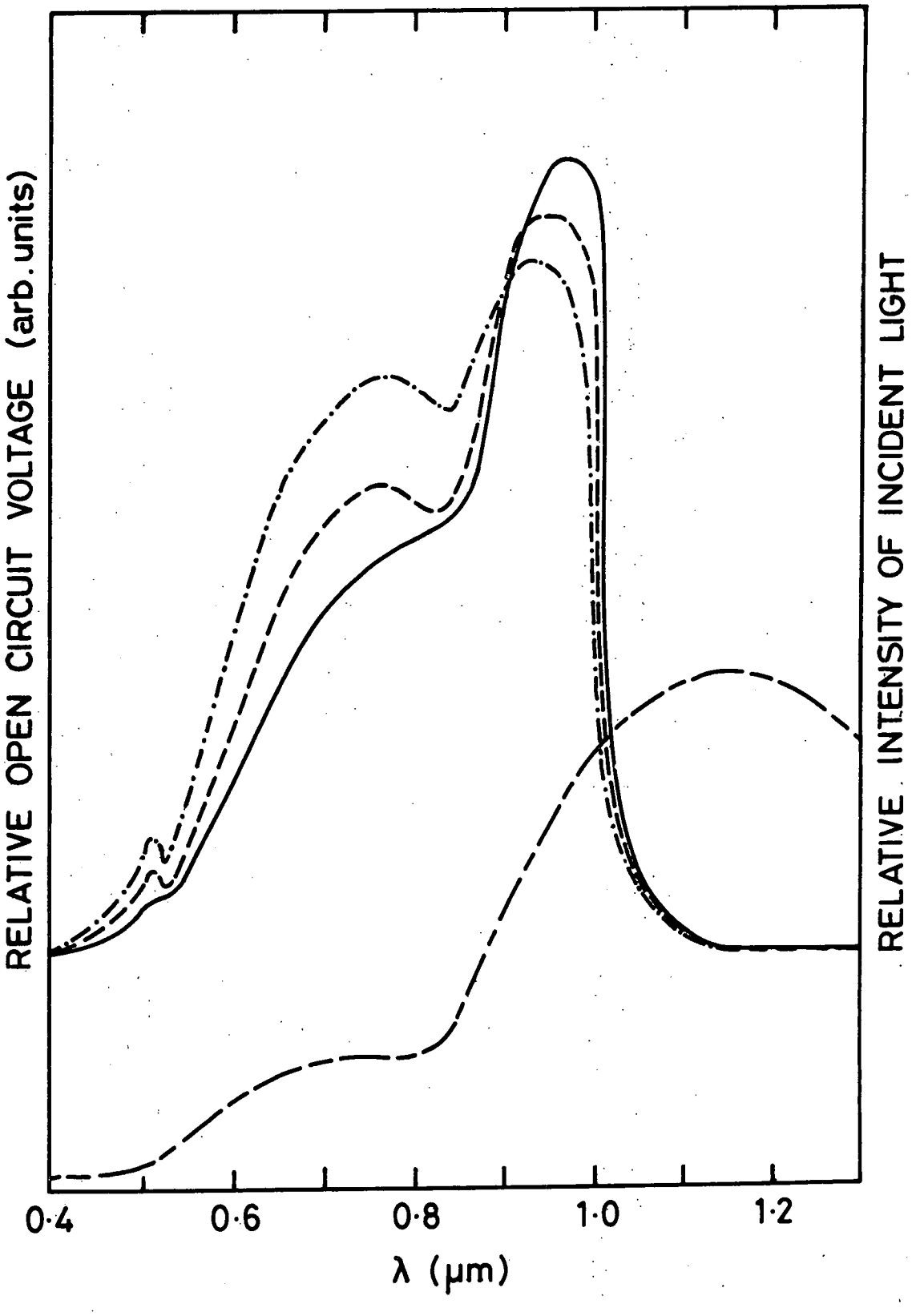


FIG.5·20. RELATIVE OPEN CIRCUIT VOLTAGES FOR AS-MADE CdS/Cu_xS CELLS CARRYING THE MIXTURE OF CHALCOCITE AND DJURLEITE

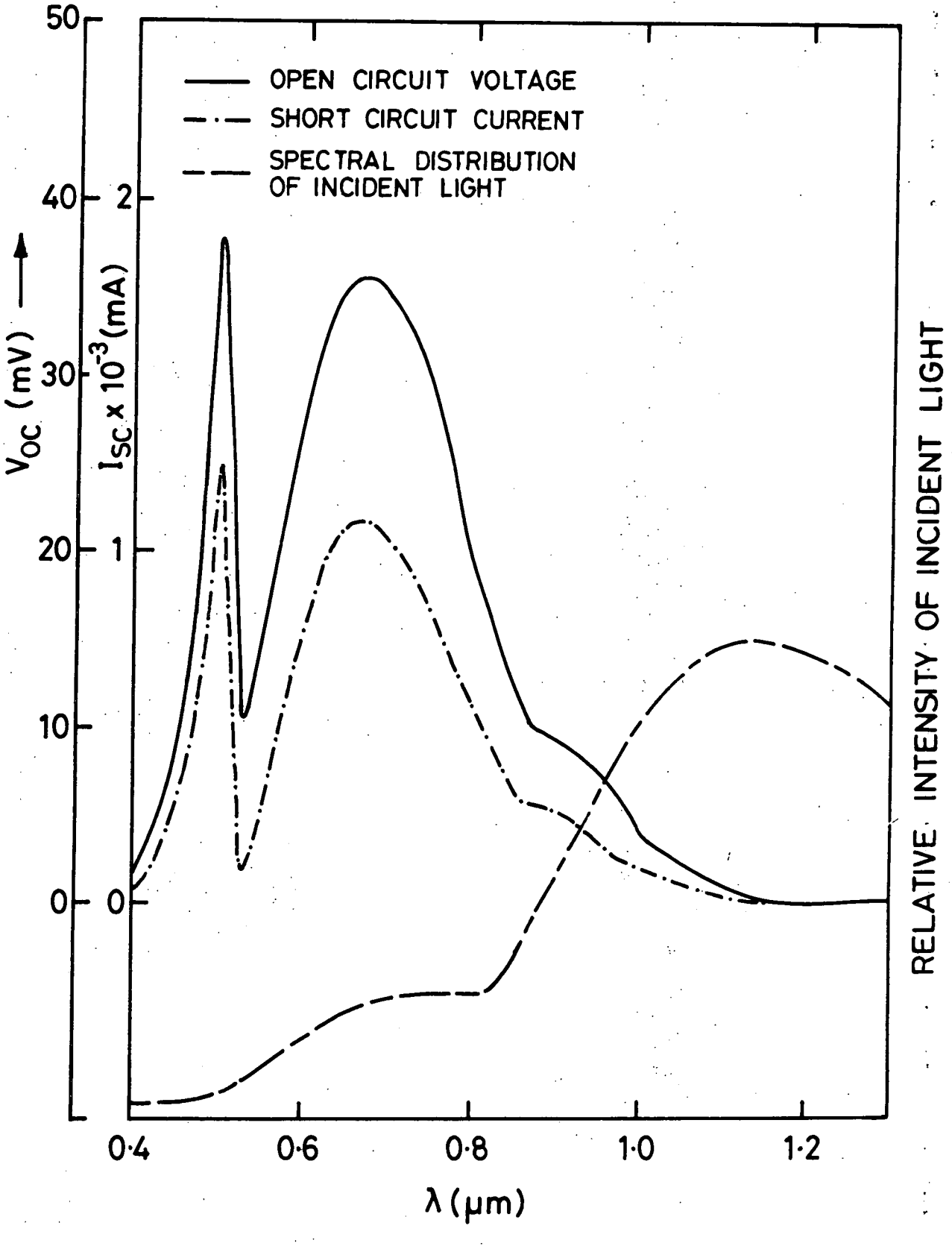


FIG.5·21. SPECTRAL RESPONSE OF V_{OC} AND I_{SC} AT ROOM TEMPERATURE FOR THE CELL CHEMIPLATED AT 85°C TO PRODUCE A LAYER OF DJURLEITE ($Cu_{1.96}S$)

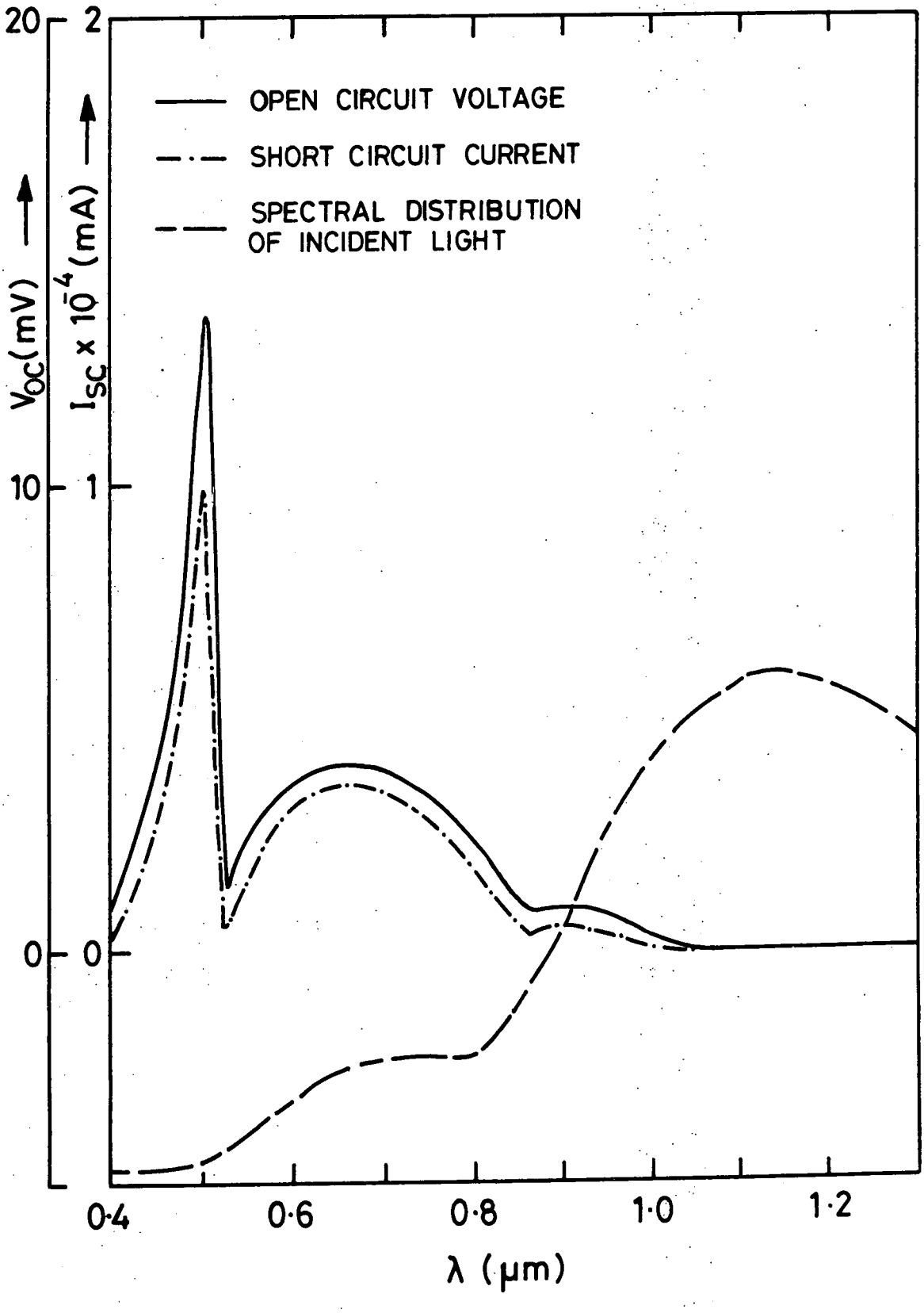


FIG.5·22. SPECTRAL RESPONSE OF V_{OC} AND I_{SC} AT ROOM TEMPERATURE FOR THE CELL CARRYING HEXAGONAL PHASE OF Cu_xS ($1·96 < x < 1·80$)

The spectral distribution of V_{OC} and I_{SC} for a cell formed at 70°C (Fig 5.22) showed that the largest response occurred in the vicinity of the band gap of CdS and there was a relatively small, broad response centred at about 0.66 μm (1.88 eV). However, there was still some sensitivity at 0.96 μm.

One further point to emphasize is that there was no significant change in the spectral responses of the as-made cells when they were additionally illuminated with green monochromatic (0.52 μm) radiation.

5.6 ANALYSIS OF CdS/Cu_xS HETEROJUNCTIONS AFTER POST BARRIER AIR-BAKE

After the necessary measurements were completed on the as-plated CdS/Cu_2S cells a "conventional" heat treatment in air was administered at 200°C for different periods. Then the effects of this treatment on the parameters of the various devices were determined.

5.6.1 Cell Performance

The results shown in Figures 5.23 and 5.24 have been obtained from type A and type B cells subjected to post barrier air-bakes at 200°C. These figures demonstrate clearly that a "conventional 2 mins post barrier air-bake" led to a very small increase in V_{OC}, and a considerable reduction in J_{SC}, in the type A cell (Fig 5.23). In contrast there was a significant improvement in the diode characteristics and the photovoltaic performance of the type B cells, Fig 5.25.

V_{OC} and J_{SC} were monitored at intervals during 4 minute air bakes at 200°C on type A and type B devices. The results are shown in Fig 5.25 (a,b,c,d). With type A devices V_{OC} under AM1 illumination remained virtually unchanged after 2 mins heat treatment. Heating for longer than 2 minutes tended to degrade the V_{OC} values, Fig 5.25(a). Conversley, J_{SC} values of type A cells decreased steadily during the heat treatment. Heating for 2 mins led to a fall in J_{SC} from 14.6 to 10.8 mA/cm^2, thereafter slow degradation continued and J_{SC} was reduced to 9.2 mA/cm^2 after 4 mins

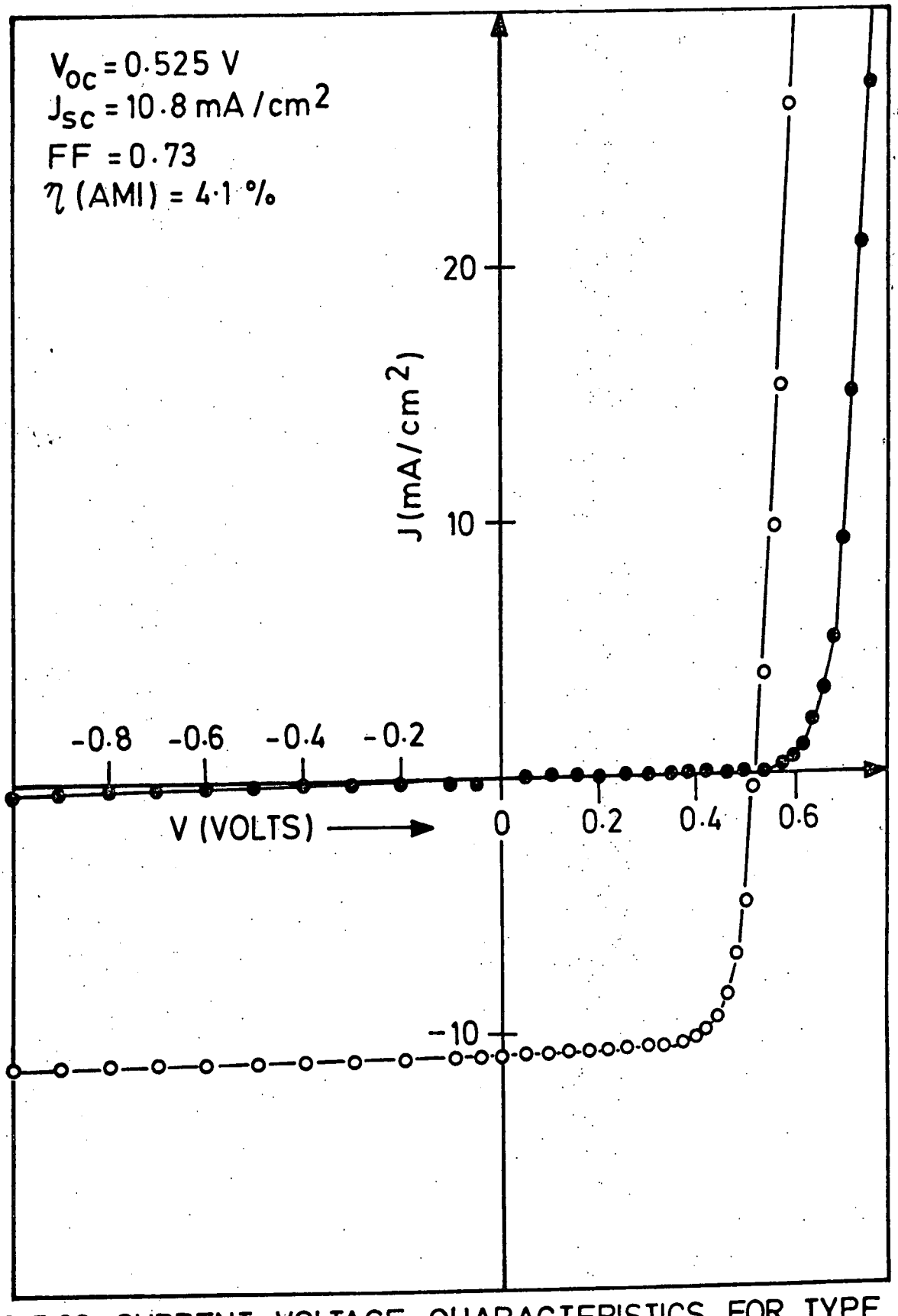


FIG.5·23. CURRENT VOLTAGE CHARACTERISTICS FOR TYPE A CELL AIR-BAKED AT 200°C FOR 2 MIN, MEASURED IN THE DARK(●)AND UNDER ILLUMINATION(○).

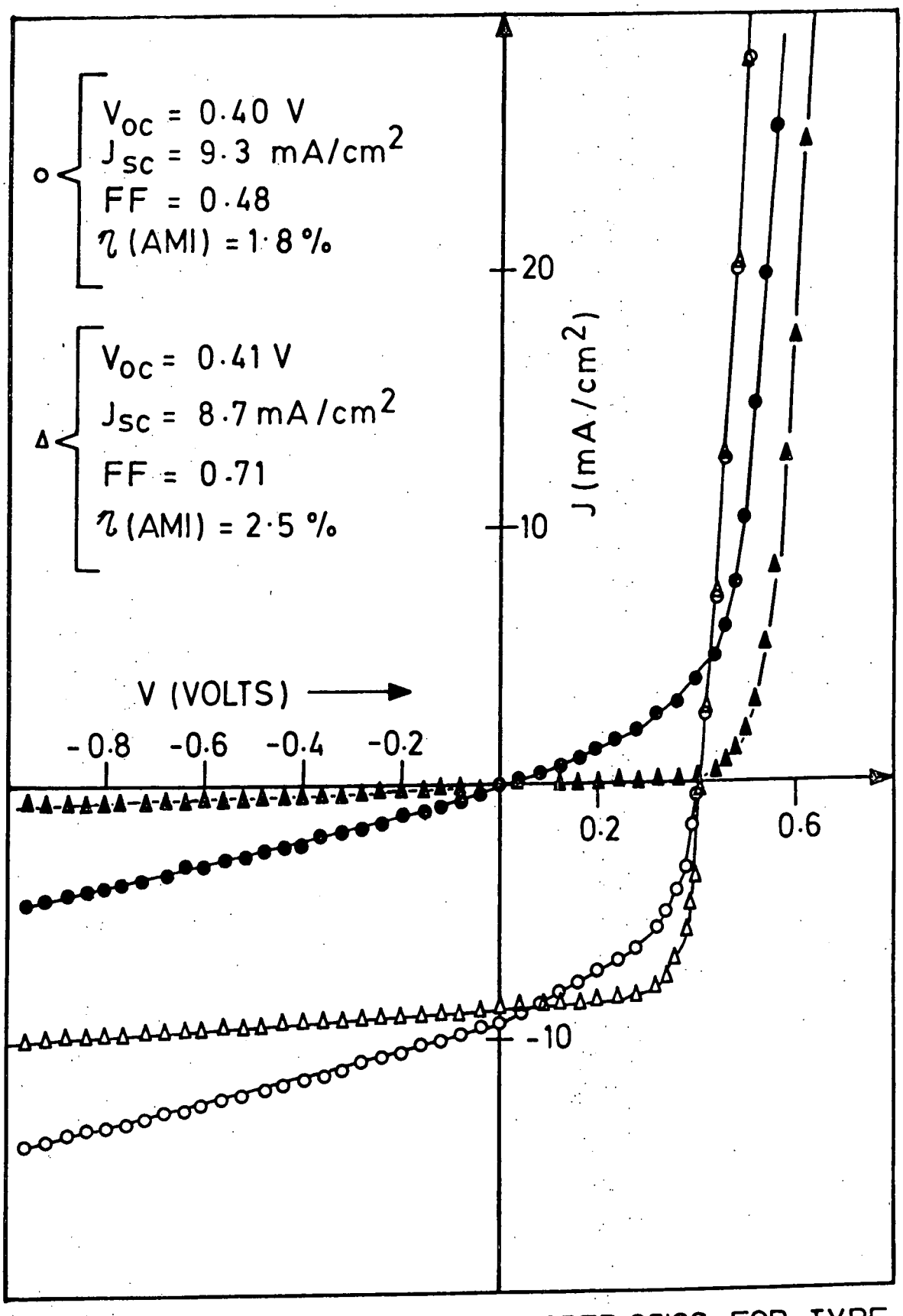


FIG.5·24. CURRENT VOLTAGE CHARACTERISTICS FOR TYPE B CELLS AIR-BAKED AT 200°C FOR 1 MIN (●/○) AND FOR 2 MIN (▲/△) MEASURED IN THE DARK (●/▲) AND UNDER ILLUMINATION (○/△).

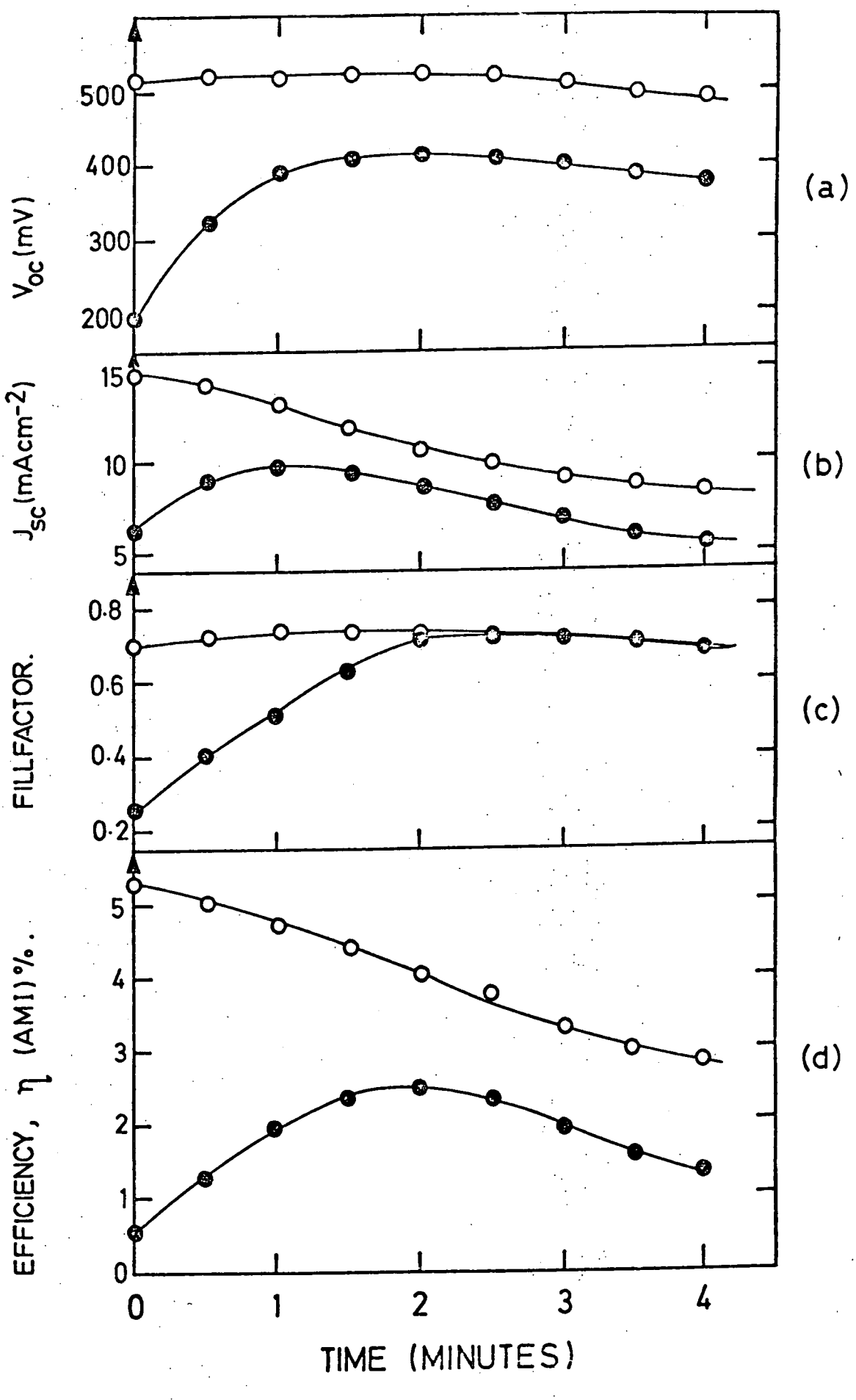


FIG. 5·25 VARIATION OF OPERATIONAL PARAMETERS WITH PERIOD OF HEAT TREATMENT IN AIR AT 200°C.
(o TYPE A , • TYPE B)

(see Fig 5.25(b). The fill factor on type A cells was not much affected by the air bake, however after 2 mins it increased from 0.69 to 0.71 and then decreased to 0.67 after a total of four minutes heat treatment, Fig 5.25(c). In summary, the overall efficiency of the type A cell shown was reduced from 5.3% to 4.1% after 2 mins of the air-bake and to 3.0% after 4 minutes, Fig 5.25(d). In contrast type B cells were improved considerably by a 200°C air bake. Figs 5.25(a) and (b) demonstrate that an initial one minute heat treatment improved the values of V_{OC} and J_{SC} from 195 mV and 6.0 mA/cm^2 tp 400 mV and 2.3 mA/cm^2 respectively. However, the gain in fill factor was not optimum for this period (from 0.25 to 0.48). A post barrier air-bake beyond one minute led first to a very small improvement and then a degradation in V_{OC}, but a significant reduction in J_{SC}. By administering post barrier air-bakes for longer periods (up to 4 mins) it was found that the optimum performance for the type B cell was obtained after a 2 mins air-bake, i.e. the fill factor increased from an as-made value of 0.25 to 0.71 and the cell efficiency η(AM1) from 0.29% to 2.5%. Thereafter although the reduction in the fill factor was almost negligible the efficiency of the cell dropped to 1.5% as a consequence of the degradation in J_{SC}.

The family of dark current-voltage curves in Fig 5.26 demonstrates that a post barrier air-bake improves the dark diode characteristic of the junctions formed on very low resistivity CdS ($\rho \lesssim 0.05\ \Omega$ - cm) which exhibited ohmic behaviour in the as-plated condition. However, although the diode behaviour of these cells can be improved drastically they gave a poor photovoltaic performance with an efficiency of only 0.7% after 2 mins air-bake (see Fig 5.27). Because of the comparatively poor photovoltaic sensitivity of these devices, they have not been investigated further. An important feature of air-baked cells was that the current-voltage characteristics of type A and B and of devices fabricated on low resistivity CdS and on polsihed surfaces measured in the dark and under AM1 illumination

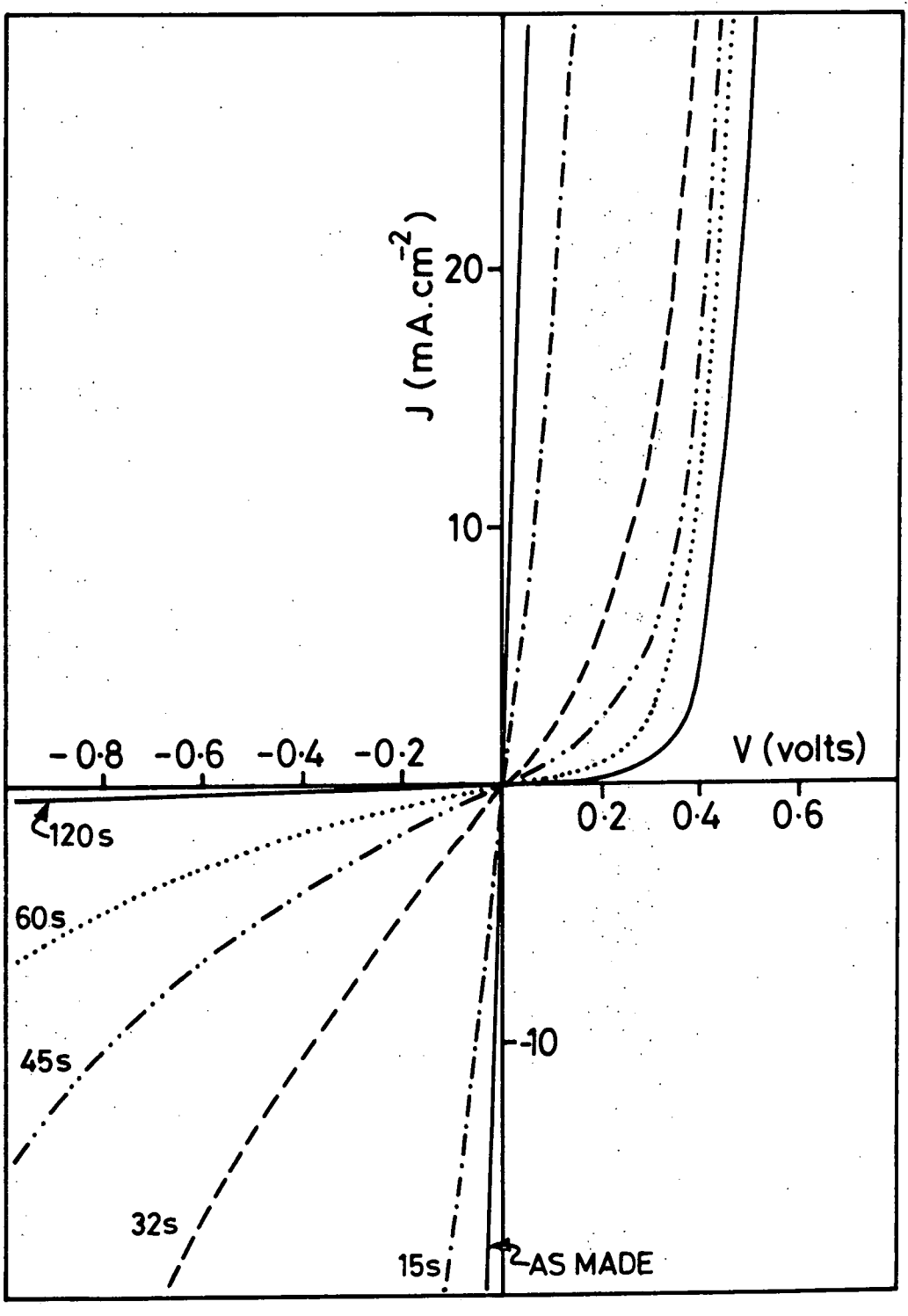


FIG.5·26. DARK CURRENT - VOLTAGE CHARACTERISTICS OF THE DEVICE FORMED ON VERY LOW RESISTIVITY ($\rho \leq 0{\cdot}05\,\Omega$.cm) CdS AS A FUNCTION OF AIR-BAKE TIME (AT 200°C)

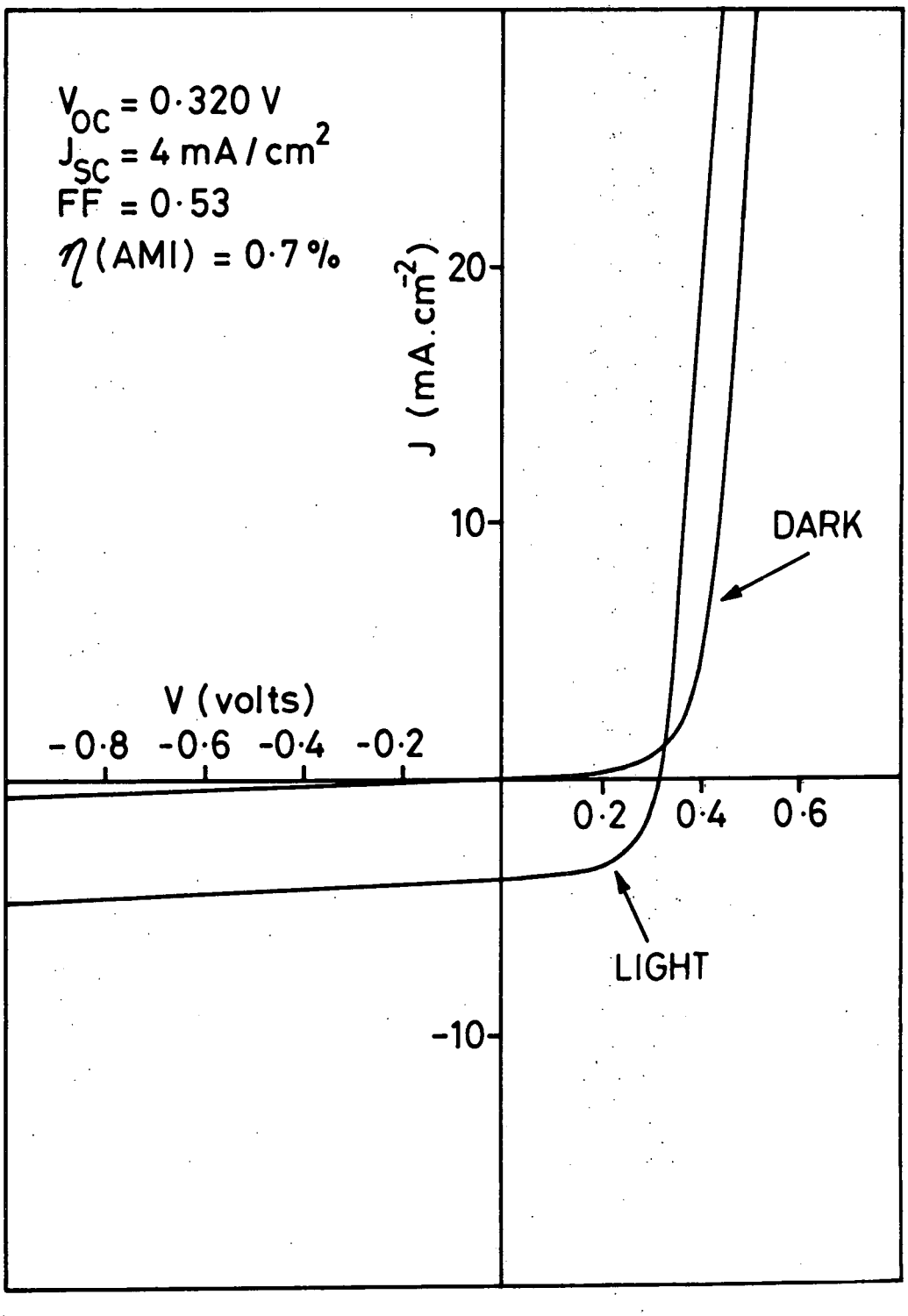


FIG.5·27. CURRENT - VOLTAGE CHARACTERISTICS OF DEVICE FORMED ON VERY LOW RESISTIVITY ($\rho \leq 0{\cdot}05\,\Omega$.cm) CdS AFTER 2 MINS. AIR-BAKE IN THE DARK AND UNDER AM1 ILLUMINATION

crossed over each other as shown in Figures 5.23, 5.24, 5.26 and 5.27, This effect became more pronounced as the period of heat treatment was extended.

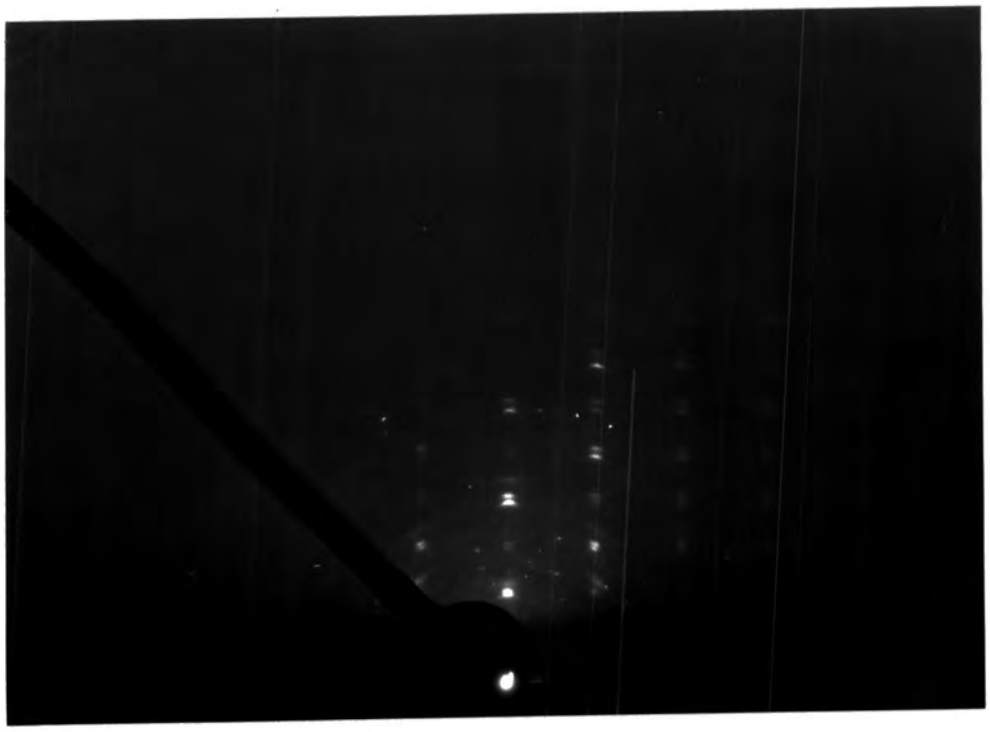
5.6.2 Phase Study (RED) After Post Barrier Air-Bake

The RED examination of devices following post barrier air-bakes at 200°C indicated clearly that phase changes occurred leading to copper deficient phases of copper sulphide. When a device with a good chalcocite layer in the as-made condition (see Fig 5.11 (a,b) was heated for 2 mins, the layer gave rise to an RED pattern similar to that shown in Fig 5.14(a) and Fig 5.14 (b) which corresponds to a mixture of a chalcocite and djurleite. As the heat treatment was extended a complete phase transformation from chalcocite to djurleite occurred. On those samples which were subjected to 4 minutes heat treatment, extra spots appeared around the more intense sublattice spots (see Fig 5.28). These extra spots were attributed to an oxidation of copper sulphide at the free surface. Further, with cells carrying a predominantly djurleite phase the heat treatment produced a transformation towards a mixture of the djurleite and hexagonal phase.

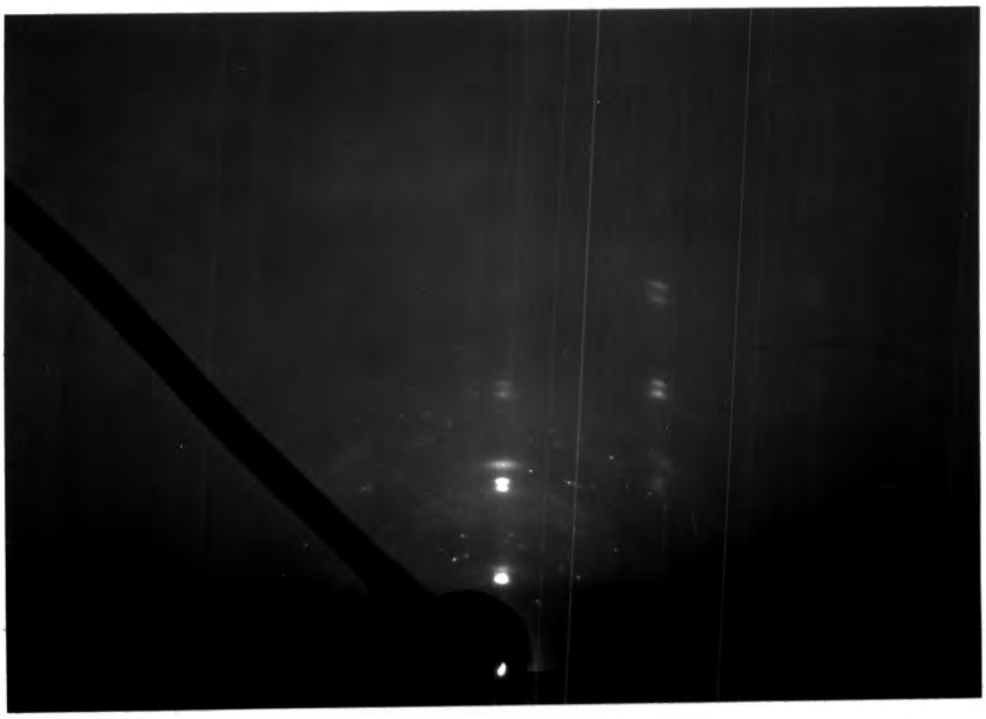
A longer period of air-baking produced a complete phase transformation to a hexagonal phase of Cu_xS $(1.96 < x < 1.8)$.

5.6.3 Spectral Response

Fig 5.29 shows the spectral response of V_{OC} for a type A cell after various periods of air baking. Curve A is for an unbaked cell carrying a layer of chalcocite. Curve B is for the same cell baked at 200°C for 30 s, showing an increase in the response at 0.7 μm and a simultaneous reduction at 0.96 μm. A marked increase in the vicinity of the CdS band gap was also apparent. Curves C and D illustrate the results of heating for one and two minutes respectively. While the relative response in the near infrared (0.96 μm) kept falling, that at 0.7 μm shifted towards shorter wavelengths and increased in magnitude. This broad response in a band near 0.63 μm had a small shoulder on the short wavelength side.



(a) "normal" orientation



(b) after a rotation of 30° about the c-axis

Fig 5.28 : RED patterns of copper sulphide layers after 4 minutes air-bake at 200°C.

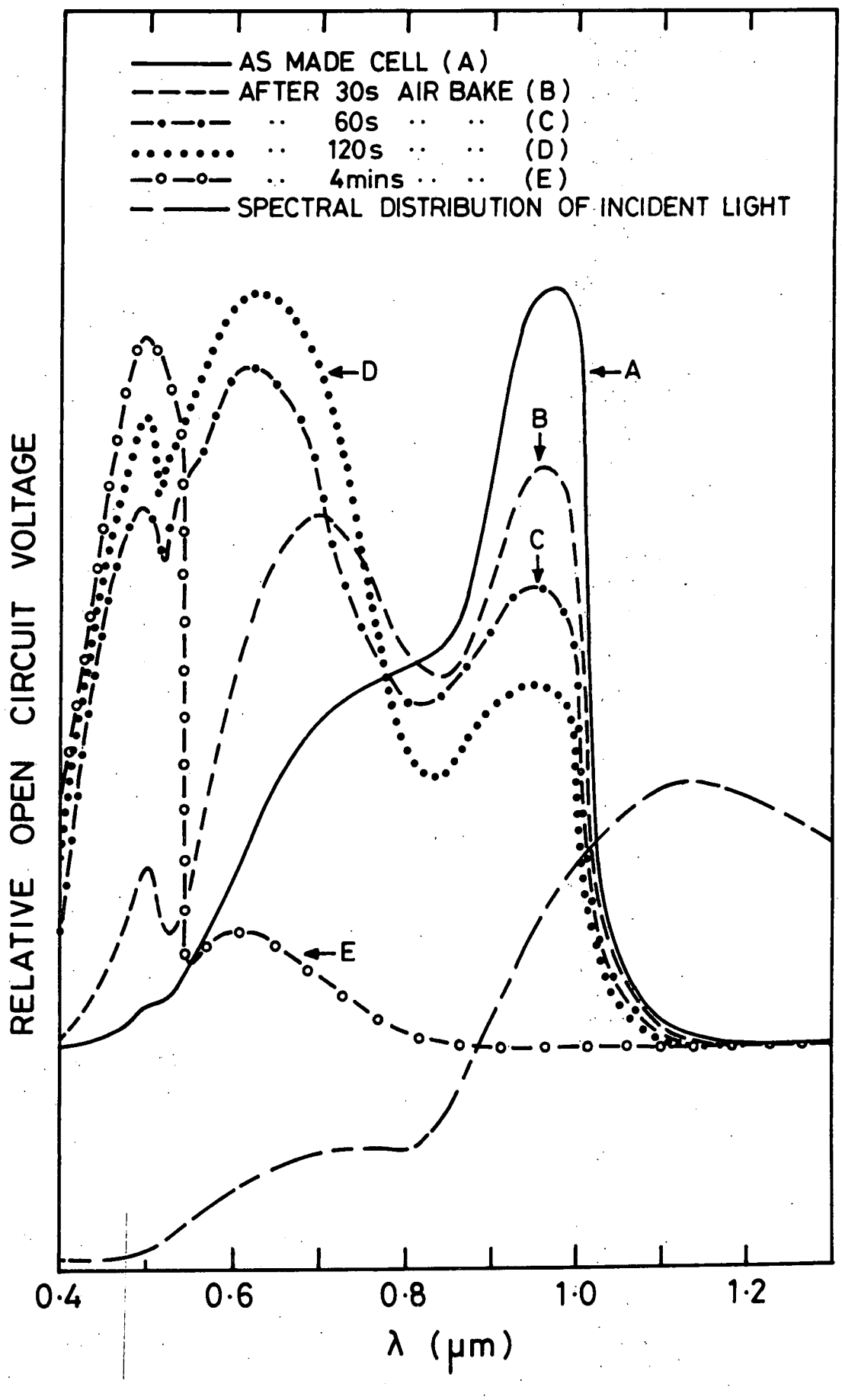


FIG.5·29. SPECTRAL DISTRIBUTION OF OPEN CIRCUIT VOLTAGE OF CdS/Cu_xS CELL AS A FUNCTION OF HEAT TREATMENT

Moreover, the relative response at the band gap of CdS became comparable in magnitude to a larger peak. When an air bake of 4 mins was administered to a type A cell, the spectral response shown as curve E was obtained. Curve E demonstrates that there was no response beyond 0.8 μm. At shorter wavelengths the sensitivity was confined to two bands at 0.63 μm and at 0.51 μm, but the relative response at 0.51 μm was much larger.

Similar changes in the spectral response of V_{OC} of a type A cell carrying a lower phase of Cu_xS were also observed. However, the replacement of the as-made spectral response curve with one resembling curve E was achieved after a shorter air-baking period.

Although the changes in the spectral distribution of I_{SC} followed a similar pattern to those of V_{OC}, the maximum peak response decreased substantially. Furthermore, the overall response of I_{SC} did not parallel that of V_{OC} closely (see Fig 5.30), as in the as prepared condition.

Heat treatment of type B cells led to a rather similar change in the spectral response pattern to that observed with type A devices. However, there was one notable difference namely that while the maximum response band moved to shorter wavelengths its amplitude increased relative to the magnitude of as-made maximum response at least for an air baking period of up to 2 mins. One further point to emphasize is that the spectral responses of baked cells were quite different when they were illuminated with a secondary bias light. The effect of the secondary illumination will be discussed in Chapter 7.

5.7 DISCUSSION OF RESULTS

The results described in this chapter show that CdS/Cu_2S photovoltaic cells on single crystal substrates can be prepared with optimum efficiency without air-baking provided they are fabricated on etched sulphur faces $(000\bar{1})$ of the CdS with the microstructural features shown in Fig 5.5 (type A surfaces), and with suitable bulk resistivity. In fact, a "conventional" post barrier air-bake at 200° C for 2 mins far from having

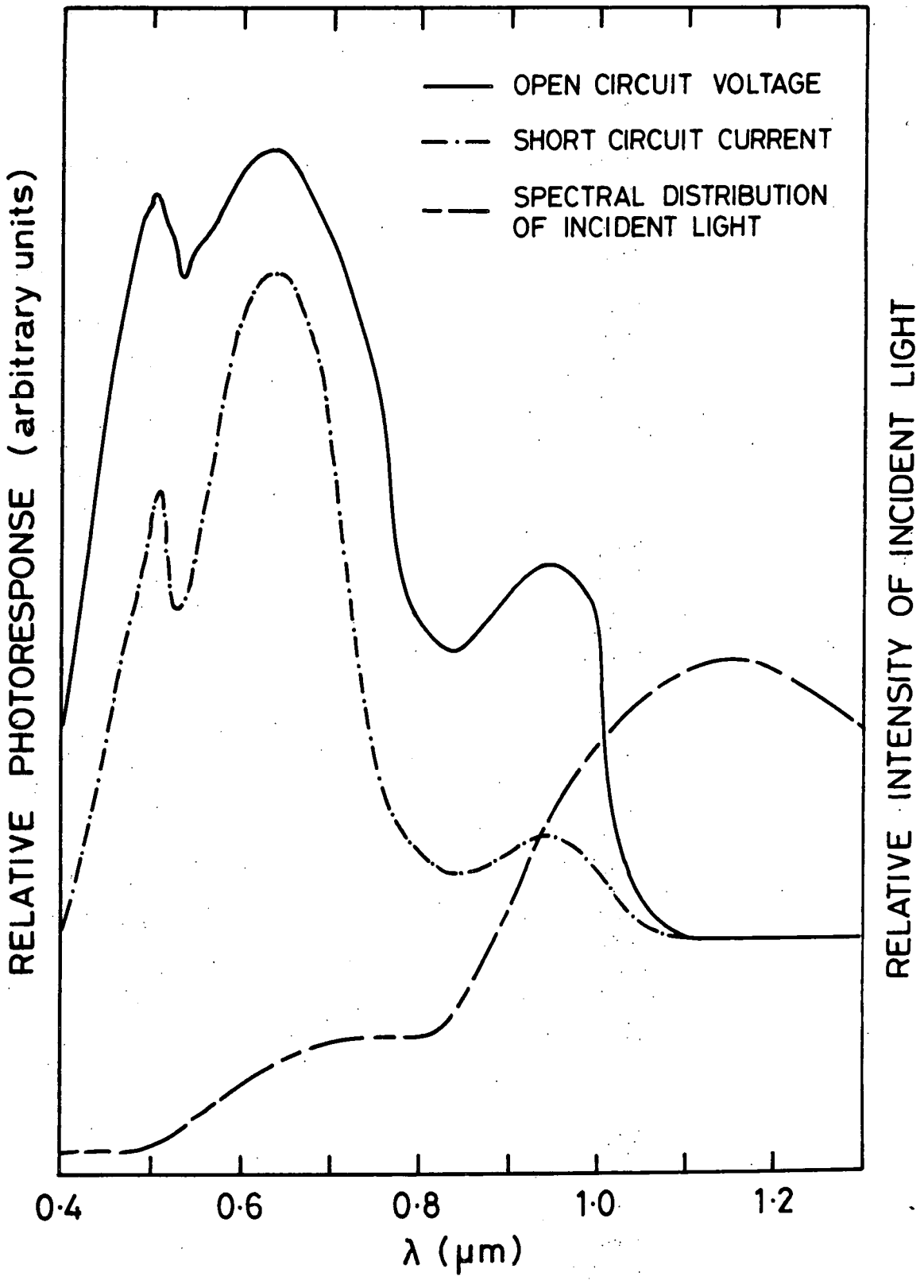


FIG.5·30.SPECTRAL RESPONSE OF V_{OC} AND I_{SC} AT ROOM TEMPERATURE FOR 2 MINUTES AIR-BAKED CdS / Cu_xS CELL AT 200°C

beneficial effects on these cells, reduces that efficiency from 5.3% to 4%, (see Fig 5.25(d)). In contrast, cells with non-optimal surface preparation (type B) or bulk resistivity which were very poor in the as-plated condition were improved dramatically after two minutes air bake, Figs 5.24 and 5.25.

In an attempt to identify those parameters associated with the considerable differences in the characteristics of type A and type B cells (see Figs 5.16 and 5.17), it is necessary to understand the importance of the following stages of cell fabrication: (1) the surface preparation prior to formation of the copper sulphide layer (2) the chemiplating process (3) the phase of the Cu_xS layer. Finally, testing and measurement of the parameters of the cell is important. When studying the effects of the mechanical polishing which was done to remove the cutting marks during the dicing, it was found that the polishing process produces a thin, polycrystalline, sphalerite cubic layer of CdS at the crystal surface (see Fig 5.1). The next stage in sample preparation is to remove the polycrystalline layer by etching in concentrated HCl. HCl is a selective etch which etches CdS in certain directions more rapidly than others. This preferential etching produces etch hillocks on the sulphur face $(000\bar{1})$ of CdS, Figures 5.5 and 5.6. However, after etching, pronounced differences were observed in the microstructural features on the sides of hillocks of samples which had been cut from hand-polished slices (type A) compared with dice cut from unpolished slices and then polished (type B surfaces). The difference may be explained as follows ; When polishing relatively large areas the polycrystalline cubic layer produced is much more uniform in thickness and in the distribution of the built-in strain etc. than it is in individually polished dice consequently the boundary between the polycrystalline layer and the underlying single crystal will be more planar and the accumulation of defects less important for type A surfaces than for type B ones. Thus as the etching proceeds

through the polycrystalline layer, HCl attacks selectively where the built-in stress and defects are concentrated[15]. The non-uniform thickness of these polycrystalline layers on type B surfaces also allows the single crystal substrates to be reached locally by the etchant in some regions before others. The RED micrograph in Fig 5.3 demonstrates the mid-stage of the etching process showing features from both the polycrystalline layer and the single crystal structure. These effects,in conjunction with expected differences in the etch rates of the polycrystalline layer and the single crystal[16], are considered to be the major factors determining the ultimate topography of the etched surfaces.

The rate of copper sulphide formation on an etched $(000\bar{1})$ surface of CdS was found to follow a simple parabolic law ($d = \sqrt{t}$) for chemiplating periods from 20 s to 300 s in duration. However, the resulting straight line does not go through the origin. Thus, the initial conversion process cannot be described by the same rule. It is thought that for short periods (<20 s) the conversion process may be controlled by an interface reaction which is a linear function of time. After a certain thickness of Cu_xS has been built up, the rate of formation becomes diffusion limited and follows a parabolic law. Nevertheless, it is assumed that the thickness of the converted layer after 10 s. chemiplating is in the range from 0.25 μm to 0.30 μm which is quite close to the measured values of minority carrier diffusion length L_n, in Cu_xS (see Chapter 6). There are conflicting reports on the growth rate of Cu_xS on CdS single crystals. Shiozawa et al[17] Lindquist and Bube[18] and more recently Kobayashi[19] described a linear time dependence, whereas Singer and Faeth[20] and Buckley and Woods[21] found that the rate of formation followed a simple parabolic law.

However, our measurements of the thickness of layers converted in the same chemiplating period, on etched or polished surfaces, revealed that the formation rate is considerably different, see Fig 5.10. These observations are at variance with those of Lindquist and Bube[18] who reported the

same growth rate for both etched and polished surfaces. However, their work was done with very thick layers and extended plating times (shortest 2 hours), so that a direct correlation might not be expected.

Moreover our work has shown that the conversion of etched CdS into Cu_xS is relatively faster on the sulphur planes. A similar conclusion was reached by Caswell et al[5]. However, there are contradictory statements in the literature. For instance, Miya et al[22] in 1970, and Kobayashi[19] in 1980 came to an opposite conclusion. The SEM images of etched surfaces of CdS given in the latter paper indicates that the identification of the Cd and S faces was in error and this may have happened with Miya et al[22]. The apparent contradictions therefore may in fact be in good agreement after the polarity correction. The observed dependence of the growth rate on the surface conditions and the crystallographic polarity offers an explanation for the non-uniform formation of Cu_xS on thin film CdS (for instance see Ref (23)) since the growth direction of some of the grains may deviate by up to 25^o from the c-axis[24].

It has been reported conclusively by several workers that the chalcocite phase of Cu_xS is the only phase yielding high conversion efficiency when combined with CdS[4,25,26]. The RED work described in this thesis was in clear agreement with this conclusion, showing that the composition of Cu_xS in good cells was dominantly chalcocite (Cu_2S). However, the correlations between the spectral response of the device and the phase of Cu_xS, using an approach similar to that described by Caswell et al[27] indicated that a small amount of djurleite ($Cu_{1.96}S$) always exists with chalcocite in the converted layer, Fig 5.19, i.e. the large response at the chalcocite band gap (0.96 μm) is always accompanied with a broad shoulder at 0.7 μm (djurleite), even though the RED patterns showed no evidence of djurleite, Fig 5.11. Before the modification of the chemiplating and drying process, the phase of Cu_xS produced under nominally identical preparation conditions was quite

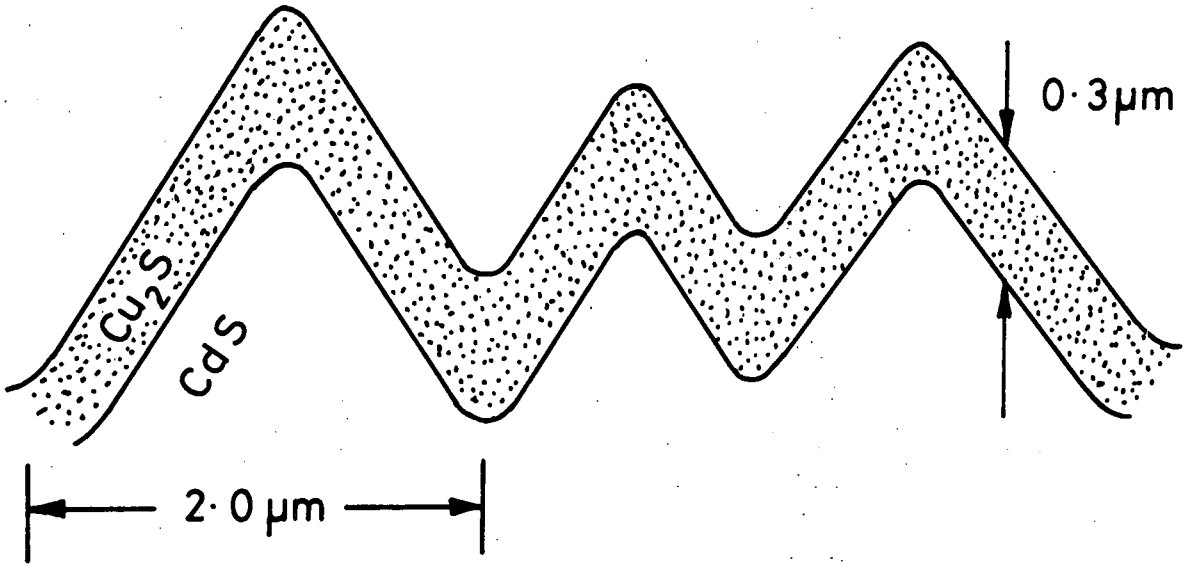
often identified by RED as a mixture of Cu_xS phases (chalcocite or djurleite dominant, $2 \leq x \leq 1.96$). The spectral distribution of V_{OC} for these devices, shown in Fig 5.20, provides strong support for a direct correlation between the phases and observed maxima in the spectral response. The frequent appearance of these different phases before the plating process was modified is attributed partly to the chemiplating itself and partly to the rinsing and drying process. The commercial CuCl (cuprous chloride) obtained was greenish in colour indicating the presence of some cupric (Cu^{+2}) ions. Thus when CuCl powder is directly added to the chemiplating bath the presence of Cu^{+2} ions causes the formation of copper defficient phases of Cu_xS. In order to avoid this CuCl was first washed in HCl to remove any Cu^{+2} ions. In addition, by etching the sample to be plated, for a short time and then preheating it in deionised water at 95°C just before immersing it in the plating bath, the problems associated with surface oxide layers and thermal inertia were eliminated. Also by rinsing with deionised water and drying in a stream of dry nitrogen some of the copper was prevented from dissolving in the methanol.

When these precautions were taken the phases produced were fully under control. After this, the RED studies of cells formed at 85° and 70°C in a plating bath demonstrated that plating at the lower temperature leads to lower stoichiometry Cu_xS (djurleite and hexagonal respectively). The spectral responses of these cells in the as-made condition were markedly different from those produced using the original plating procedure. In the spectral distribution of the djurleite samples the peak responses at 0.69 and 0.52 μm are associated with optical absorption in the djurleite and in the underlying CdS respectively, Fig 5.21. The spectral response of cells produced by chemiplating at 70°C indicated that the absorption of light in hexagonal Cu_xS then occurs at shorter wavelengths (0.63 μm) and the response at 0.52 μm becomes relatively large. The spectral response in the vicinity of the CdS band gap increases on going from chalcocite Cu_2S to

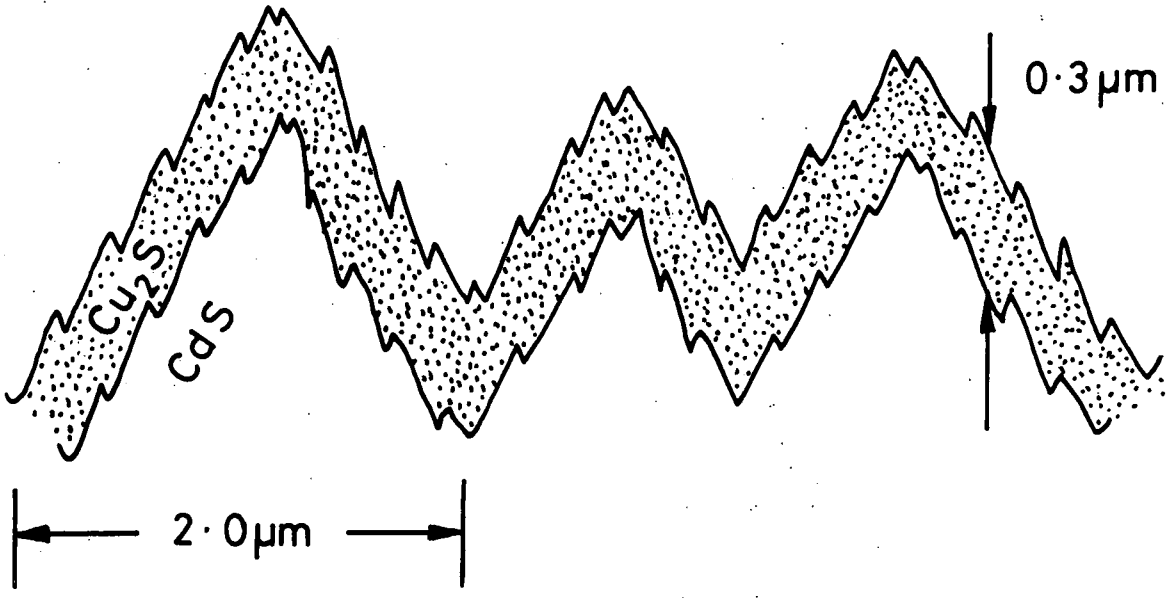
djurleite, $Cu_{1.96}S$ to hexagonal Cu_xS ($1.96 \lesssim x \lesssim 1.8$), indicating that the intensity of the light reaching the underlying CdS increases. This can be partly attributed to a decreasing absorption coefficient with increasing copper deficiency[26], and although the samples were chemiplated for longer periods at the lower temperature, can be partly associated with the decreasing thickness of the converted layers[14].

The spectral response is determined by the number of electron hole pairs generated in the Cu_xS and the CdS and the interface collection factor (for details on the interface collection factor, see Chapter 3, section 3.7.1). Type A and type B cells with chalcocite layers approximately 0.3 μm thick had negligible contributions from the CdS in their as-made conditions, Fig 5.19. Thus for these cells virtually all the current was photo-generated in the Cu_2S, so that the magnitude of the light generated current, j_{LO} is determined by the intensity and wavelengths of the incident light and the properties of the Cu_2S layer, such as the thickness, the minority carrier diffusion length and the absorption coefficient. Measurements made here showed that the thickness and the phase, which determines the absorption coefficient, of Cu_xS layers on type A and type B devices were the same, and the spectral responses recorded for both were of similar shape although there was a considerable difference in magnitude. Moreover the diffusion length, L_n measured in the Cu_xS did not indicate any significant difference either (see Chapter 6). Thus it is suggested that the density of electron-hole pairs created under defined illumination is the same for type A and type B devices but there is an immense difference between their collection efficiencies and this is the root of the differences in the operational parameters. With cells with the lower stoichiometry of Cu_xS the spectral response curves for type A and type B devices were also similar but now the contribution from CdS was comparable to the response from Cu_xS. The spectral response of a device irradiated with bias light (white or 0.52 μm monochromatic) showed

the same spectral features with the curves simply displaced. This suggests that neither the intensity nor the wavelength of the light reaching the CdS modulates the interface collection efficiency in as-made devices. Since it has been assumed that the light generated current density j_{LO} is similar for type A and type B devices, differences in the cell performances must be attributed to differences in the recombination paths through interface states (this will be discussed in detail in Chapter 7). The examination of large numbers of type A and type B devices in the secondary emission mode in the SEM demonstrated that there is a direct correlation between the surface features and the operational parameters of a cell. A similar relationship has been observed by Shirland[15] and by Norian and Edington[24] for thin film CdS/Cu_2S devices. However, the complexities of grain boundaries and different grain orientations[24] in thin films do not allow a correlation to be made between device characteristics and specific surface features as has been done with single crystal in this research. In Chapter 6 it will be shown that kink sites and steps on the sides of etch hillocks lead to a higher local density of interface states when a barrier is formed on these features. By extending this to include the entire surface of type B device with many kink sites on all of the hillocks, Fig 5.6, the interface betweeen CdS and Cu_2S is expected to be similar to that drawn schematically in Fig 5.31(b), whereas for cells formed on type A surfaces with an array of smoothly facetted hillocks, (see Fig 5.5) the interface will be as shown in Fig 5.31(a). Although it is not easy to measure the interface parameters of CdS/Cu_2S heterojunctions, the situation may be summarised as follows : with type B devices numerous ledges and kink sites on hillocks result in a higher local interface state density which gives rise to correspondingly higher interface recombination velocity, S_I (see Chapter 3, Eq. 3.8) ; such a change in S_I will affect the interface collection factor directly. Further, in the case of a high density of interface states, the probability of tunnelling to



(a)



(b)

FIG. 5·31 SCHEMATIC MODEL OF THE JUNCTION CROSS SECTION (a) AT TYPE A SURFACE (b) AT TYPE B SURFACE

these states will be very high and as a consequence the effective barrier and related electric field in CdS will be quite low, which again directly influences the interface collection factor. So most of the light generated current j_{LO} in the type B cell, which crosses the junction from Cu_2S to CdS returns to the Cu_2S via the interface states and the measured J_{SC} appears to be very low. In the dark, electrons with low energy tunnel from the conduction band of the CdS into empty interface states then recombine with holes in the valence band of Cu_xS, or holes tunnel from the Cu_xS valence band into occupied states in the CdS then recombine with electrons. As a result type B devices have very poor rectification and a high leakage current in their as-made condition. In addition, the achievable V_{OC} and the effective barrier is limited as Fig 5.17 shows.

Following this argument the junction formed on type A surfaces, Fig 5.5, would be expected to have a much lower denisty of interface states which then, would arise mainly from lattice mismatch. This is indeed confirmed by the excellent rectifying behaviour, photovoltaic performance, and the small reverse leakage current of as-prepared type A devices, Fig 5.16.

For cells directly formed on polished surfaces of CdS, the cross-over effect and light-induced breakdown in the as-made condition are thought to be associated with the underlying polycrystalline layer of CdS which is photoconductive. However, these effects disappeared after longer periods of chemiplating which is a consequence the conversion of the whole polycrystalline layer to Cu_xS, as can be seen in Fig 5.18. The ohmic behaviour of devices fabricated on very low resistivity substrates ($\rho \lesssim 0.05$ Ω -cm) in their as-made condition, regardless of their surface features, indicates that the tunnelling probability is too high in cells with too narrow a depletion region in the CdS. A similar effect has been reported in thin film CdS/Cu_2S devices by Hall and Singh[28].

When a post barrier air-bake is administered, it is generally accepted that copper diffusion occurs from the Cu_2S into CdS leading to donor compensation in the CdS to a certain depth[17,28,29]. While copper diffuses into CdS,

another effect of air baking is to allow the diffusion of oxygen to the junction interface, where it forms electron traps[30]. Further, Deb and Saha[31] suggested the possible appearance of a thin insulating layer between the CdS and the Cu_xS with the gradual improvement of the barrier in CdS with increasing duration of the air-bake. On the other hand, migration of copper from the Cu_xS to the CdS increases the density of Cu vacancies in Cu_xS. Cu vacancies act as acceptors, hence the hole density and the position of the Fermi level are determined by these vacancies. A change in the stoichiometry and the sheet resistance of Cu_xS following a post barrier air-bake to lower values is also well established[32,33]. By taking these effects in account, in conjunction with the discussion of the as-plated cell, the changes in the rectifying behaviour and in the operational parameters of type A, type B cells following a post barrier air-bake can be interpreted qualitatively as follows : first the barrier height of type B devices, which is low, improves as oxygen is absorbed at the interface, and secondly the width of the tunnelling distance increases following the diffusion of copper and the resulting compensation. Thus the dark current-voltage characteristics of type B and low resistivity based cells improve with increasing duration of the air-bake. Since the barrier height and the related electric field become progressively greater, and the interface recombination velocity smaller, the light generated electrons which cross the junction will have a higher probability of being collected than recombining via interface states (high interface collection factor). Hence, the photovoltaic properties of type B devices improve. On the other hand, the stoichiometry changes introduced by heat treatment reduce the light generated current drastically as a consequence of the reduction in the sheet resistance[13] and the absorption coefficient[4]. Recently, the theoretical calculations by Rothwarf and Windawi[34] indicated that a change in sheet resistance by a factor of 10 results in a 20 to 40% change in J_{SC}, and they

also demonstrated that the experimental absorption data for Cu_2S follows a similar trend. Although neither the absorption coefficient nor the sheet resistance of the Cu_xS layer has been studied in this work, RED examination and spectral response measurements have shown that the chalcocite tends to copper deficient phases after a post barrier air-bake, Figs 5.28 and 5.29. So that while the light-generated current decreases significantly, the interface collection factor of type B devices increases and the corresponding value of J_{SC} rapidly reaches a maximum, Fig 5.25(b), before falling after the interface collection factor reaches its optimum. If the heating in air is prolonged after V_{OC} reaches a maximum, copper diffuses deep into the bulk and reduces the achievable built-in voltage and of course reduces V_{OC}, Fig 5.25(a). The competition between these effects yields the optimum efficiency of type B devices after two minutes of air-baking, Fig 5.25(c). It is clear that as the barrier height increases and the tunnelling current (shunt current) decreases the fill factor also increases significantly. Although heat treatment obviously plays an important role for type B cells, if the cells had been prepared with a high interface collection factor and good diode characteristics in the first place, the effects of heat treatment are undesirable. The notable consequences of post barrier air-baking on type A cells are that V_{OC} and the fill factor are not changed significantly Figs 5.25(a) and (c), but J_{SC} decreases considerably, Fig 5.25(b), and the efficiency of a cell follows the deterioration in J_{SC}, Fig 5.25(d).

Further, the existence of a cross-over effect between the current voltage curves measured in the dark and under illumination for all devices, is explained by the formation of a compensated layer in the CdS with distinct photoconductive properties. The photoresponse of heat treated devices can be regarded as the generated current modulated with the behaviour of the compensated layer. The band gap of Cu_xS increases with increasing duration of the air-bake, but a simple correlation between the phase of Cu_xS

and the spectral response is no longer valid, because the current collected at each wavelength also depends on the intensity and wavelength of light reaching the compensated layer.

5.8 CONCLUSIONS

In the preparation of CdS/Cu_xS photovoltaic cells, there have been many reports indicating that a post barrier air-bake is an essential step in producing optimum efficiency[5,6,13,17,18,25,28,35,36,37]. Many authors with some exceptions[18,35] found that their unbaked cells exhibited little rectifying behaviour and photovoltaic sensitivity. The work described in this chapter shows that a post barrier air-bake is essential to improve the characteristics and performance of cells which have poor operational parameters in their as-plated condition (type B). However, for cells with good characteristics and performance in their as-made state (type A) there is no advantage to be gained from an air-bake. In fact undesirable effects of the air bake degrade the performance of these cells. Thus when CdS/Cu_2S single crystal photovoltaic cells are prepared under controlled optimized conditions, which involve the surface preparation and the bulk resistivity of the CdS and the correct stoichiometry and thickness of the Cu_xS layers, the cells will have their optimum efficiency in the as-prepared condition and their stability will be good.

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CHAPTER 6

ELECTRON BEAM INDUCED CURRENT (EBIC) STUDY OF CdS/Cu_2S SINGLE CRYSTAL CELLS

6.1 INTRODUCTION

A detailed microscopic study of the CdS/Cu_2S heterojunction forms the main topic of this chapter. This has been carried out using a scanning electron microscope in the electron beam induced current (EBIC) mode. A description of the capability of the SEM has already been given in Chapter 4. Section 6.2 includes a discussion of the interaction of an electron beam with matter and of the EBIC process particularly in CdS/Cu_2S heterojunctions. The next section is concerned with an examination of type A and type B devices before and after a post barrier air-bake to gain insight into the correlation between the ultimate behaviour of cells and their surface features. This was accomplished by operating the SEM in the stationary spot mode and measuring the I-V characteristics with the beam incident on the areas giving contrasting EBIC images. In section 6.5 the measurement of minority carrier diffusion lengths in the CdS and in the Cu_2S are described for as-prepared and heat treated samples.

6.2 ELECTRON BEAM INDUCED CURRENT (EBIC)

If a p-n junction is placed in close proximity to a focussed electron beam, carriers created by the incident electrons are collected after diffusion to the junction and can produce an induced current in an external circuit. This technique, exploited in the scanning electron microscope (SEM), is called the electron beam induced current (EBIC) mode and is widely used to obtain quantitative information about semiconductor devices or about the physical properties of a semiconductor material. Before discussing the mechanisms of the EBIC image contrast, it is desirable to have a general picture of electron interaction with solids. There is an

extensive literature on this topic from which it is apparent that the interaction is qualitatively the same regardless of the target material[1].

When a semiconductor is bombarded with electrons with energies in the range 1-50 keV, the interaction is very complex. The primary effects on the electrons of the high voltage incident beam are :

(1) elastic scattering which is caused mainly by interaction with the nucleus when a significant deviation from the incident direction occurs ;

(2) inelastic scattering by interaction with both the atomic nucleus and the bound electrons.

It is common to think of the elastic scattering process as occurring in two parts : (a) Rutherford scattering which occurs in the Coulomb field of the nucleus and (b) multiple scattering ; when the electron passes through the electron cloud of an atom which screens the field of the nucleus small-angle scattering occurs.

A thorough treatment of the dissipation of the energy of an electron beam during inelastic scattering in a solid is very complicated, but the dominant process will be the excitation of both strongly bound core electrons and more loosely bound valence electrons. The first type of excitation results in the emission of x-ray radiation (photons) and Auger electrons. Energy analysis of x-ray photons and Auger electrons allows identification of the elemental composition of bulk material and the surface of the sample respectively (for details see Refs (2), (3)). Most of the dissipated energy, however, does not escape from the specimen through the emission of photons and electrons, and roughly a third of this energy will ultimately be dissipated to produce electron hole pairs, with the rest being dissipated as heat[4]. The average energy required to create a single pair is called the radiation-ionization energy, e_i, and is roughly about three times the band gap energy, Eg[5].

The depth at which primary electrons have dissipated all their energy, is called the total range R, and the rate of energy loss in a

plane perpendicular to the beam axis is referred to as the Depth-Dose function. Direct correspondence between the rate of electron-hole pair generation and the rate of energy loss by the electron beam can be used to determine the spatial distribution of electron beam induced minority carriers[6,7]. Spencer[8] first developed the theory of the Depth-Dose function. Then the experimental evidence for the scaling of this function to the primary electron range was given by Gruen[9]. A common assumption is that the shape of a Depth-Dose curve is not a function of either the incident energy or the target material and has the shape shown in Fig 6.1. The maximum energy dissipation occurs some distance below the surface and is followed by a rather straight line descent to the final tail of the distribution. The Gruen range R_G, is defined by the extrapolation of the straight part of the curve to zero, and the depth at which the curve tails off is defined as the Bethe range R_B (see Fig 6.1). Everhart and Hoff[10] have proposed "a universal curve" of energy dissipation as a function of normalized electron energy in an expression of the form

$$R_B = k E_o^{\alpha} \tag{6.1}$$

They derived this expression from Bethe's theory. In Eq. 6.1 E_o is the primary beam energy while k and α are coefficients determined by the average atomic number, $\bar{Z}$, average atomic weight and the mass density ρ of the material. Shimizu et al[11] have made calculations of the energy-range relations in Al, Cu, and Au. Their simulations are Monte-Carlo calculations, which are in a good agreement with the Everhart and Hoff curves[10]. Shea et al[12] have given an accurate range-energy relation for CdS and Cu_xS by using a ratio of $\frac{R_G}{R_B} = 0.81$ and the Everhart and Hoff

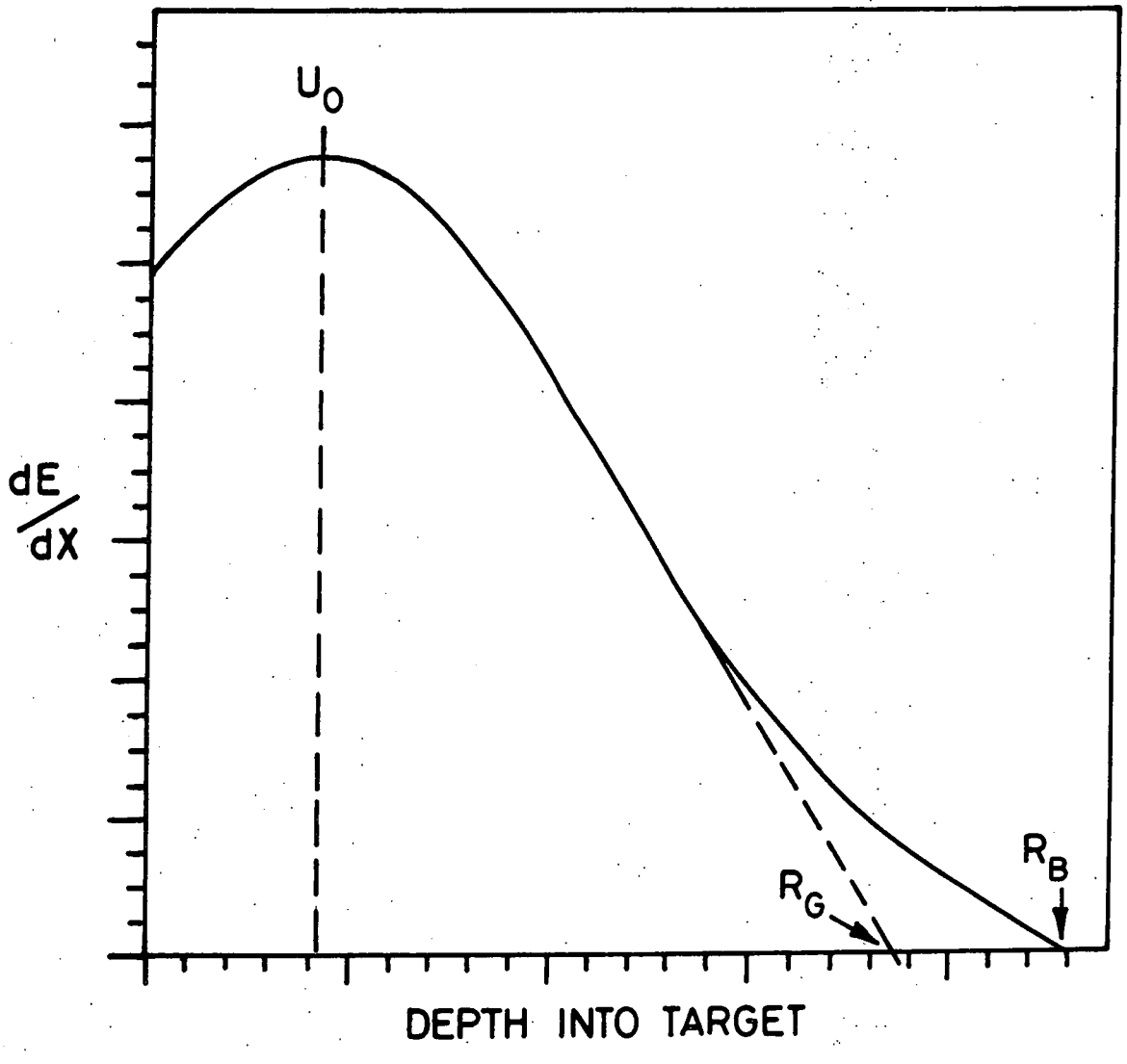


FIG. 6·1 TYPICAL DEPTH - DOSE FUNCTION (Arbitrary Scales) REF. [23]

expression.

$$R_G\ (Cu_xS) = 0.015\ E_o^{1.62}\ \mu m \qquad 3 \leq E_o < 20\ kV$$
$$R_G\ (CdS) = 0.021\ E_o^{1.62}\ \mu m \qquad (6.2)$$

and

$$R_G\ (Cu_xS) = 0.015\ E_o^{1.78}\ \mu m \qquad 20 < E_o < 30\ kV$$
$$R_G\ (CdS) = 0.021\ E_o^{1.78}\ \mu m$$

Shea et al[12] and Pfisterer et al[13] have measured the effective generation depth, d, in CdS/Cu_xS structures, and by comparing d with R_G, they found a relationship of the form $d = 0.5\ Rg$. Shea et al[12] have also measured the Lateral-Dose function on single crystal CdS/Cu_2S heterojunctions. They defined the Lateral-Dose function as the energy dissipation per unit distance from the axis of the beam which was taken to be a Gaussian distribution with a lateral range energy relation of about $0.25\ R_G$. In fact this is the function of interest in diffusion length experiments and limits the accuracy of the diffusion lengths measured.

In the range described above, the number of pairs created by one incident electron with energy E_o is E_o/e_i where e_i is the radiation ionization energy. If I_b is the total current of primary electrons and δ, the fraction of backscattered ones, the rate at which electron hole pairs are created is

$$G_T = \frac{I_b E_o}{e_i}\left(1 - \frac{\delta E_{BS}}{E_o}\right) \qquad (6.3)$$

where E_{BS} is the energy of the back-scattered electrons and has the value $(0.45 + 0.0002\ \bar{Z})E_o$ for values of E_o between 0.2 keV to 30 keV[14].

Any change in the generation and collection efficiency of the carriers produced will lead to contrast in the EBIC image as the beam scans the sample. Since the SEM can provide a beam less than 300 Å in diameter. The EBIC technique proves a powerful tool to investigate the

correlations between the parameters of devices, and to measure the diffusion lengths of minority carriers within certain limits. The experimental arrangement for the formation of EBIC images and the measurement of diffusion lengths is shown schematically in Fig 6.2. The sample is mounted in the specimen chamber of the SEM with separate connections to both the back and the top contact. By changing the appropriate parameters such as the energy or angle of the incident beam, and the biasing condition, the possible sources of EBIC contrast can be investigated.

6.3 STUDY OF EBIC IMAGES AND LOCAL SENSITIVITY IN AS-MADE CdS/Cu_2S

As explained in Chapter 5, the etched $(000\bar{1})$ plane of a CdS crystal is characterized by an array of etch hillocks. The existence of extra features such as ledges and kink sites on these etch hillocks depends strongly upon the method of surface preparation. Devices formed on surfaces with uniform smoothly facetted hillocks will once again be called type A (Fig. 6.3),whereas devices on surfaces with hillocks with numerous kink sites and ledges will be referred to as type B (Fig 6.7). In Chapter 5 it was shown that as-prepared type A cells have good diode characteristics and high photovoltaic performance. In contrast, type B cells have poor rectifying and photovoltaic characteristics. In an attempt to determine whether there was a correlation between surface features and the operational parameters of a cell, the EBIC image contrast and the localised microscopic photovoltaic sensitivity of type A and type B cells have been studied in more than 40 devices carrying either chalcocite and djurleite layers of copper sulphide in their as-prepared state. When as-made type A cells were examined in the EBIC mode with 7.5 keV beam energy (Fig. 6.4) and zero bias, light EBIC contrast was observed along the sloping sides of the hillocks (occasional dark spots were located in the midst of the light regime), dark EBIC contrast was apparent on the summits of the conical hillocks, and along the valleys at the boundaries between hillocks. In addition there was faint EBIC contrast at the edges

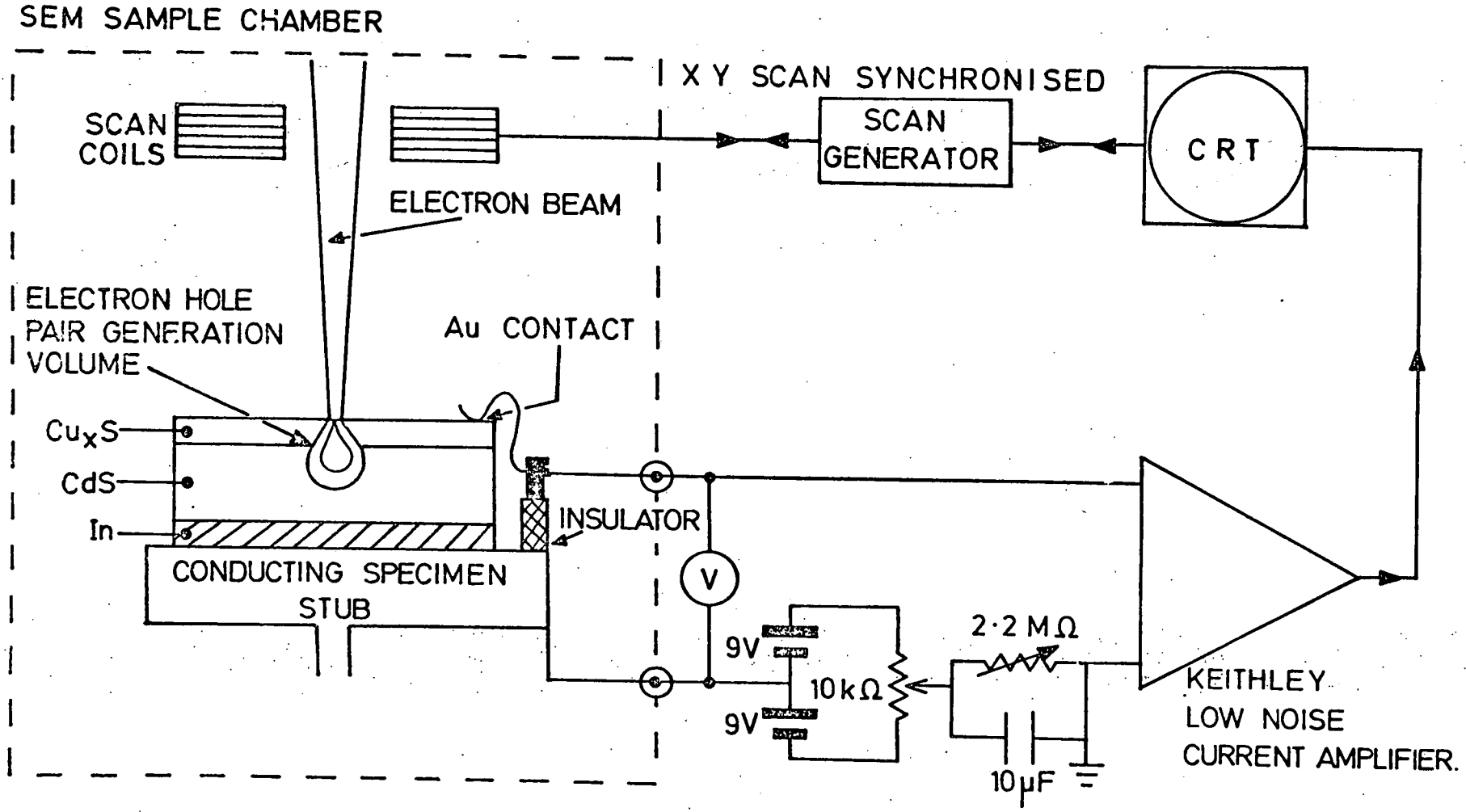


FIG. 6·2 THE EXPERIMENTAL ARRANGEMENT FOR E B I C STUDY

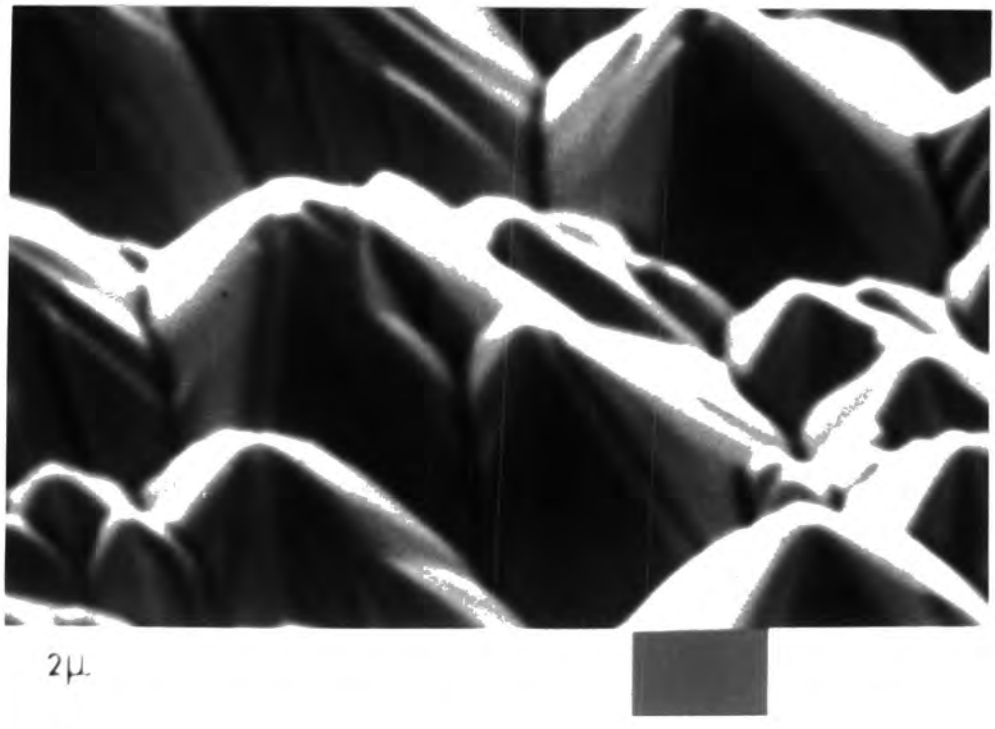


Figure 6. 3 : Secondary Emission micrograph of CdS/Cu_2S type A device surface.

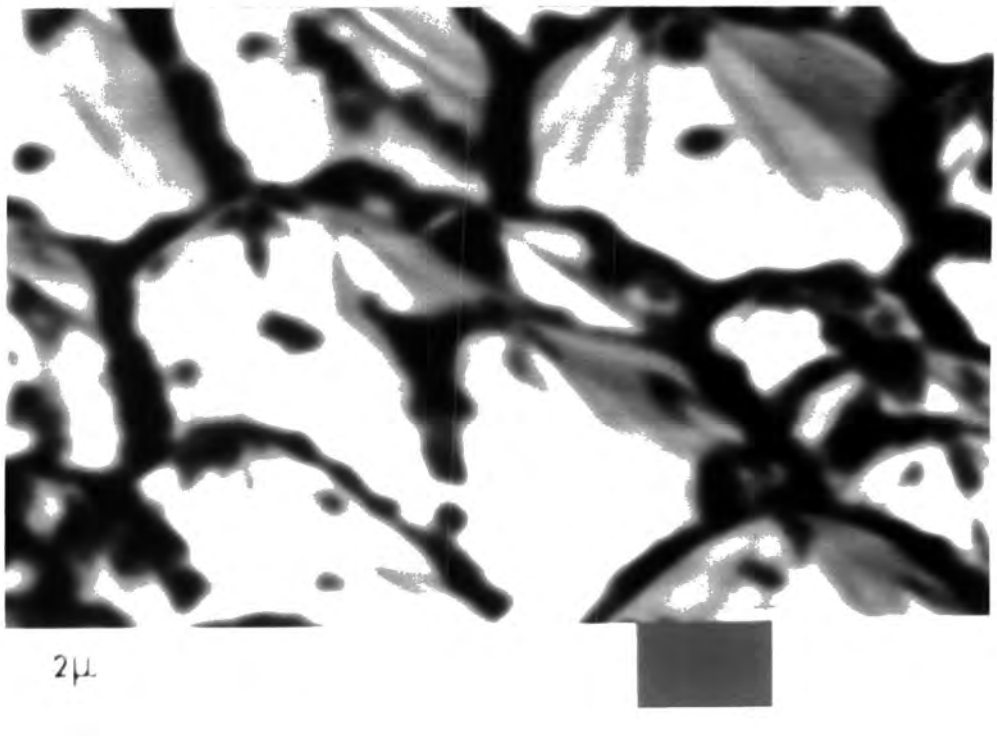


Figure 6.4 : Electron Beam Induced Current image of the type A device shown in Fig 6.3 (E_o = 7.5 keV).

of facets. The contrast did not change when the energy of the incident beam was increased to 25 keV (Fig 6.5 and 6.6) although the resolution improved. It was qualitatively obvious that the total area of dark contrast was a small fraction of the total surface area of all type A cells.

An SE micrograph and corresponding EBIC image for an as-prepared type B cell are shown in Figs 6.7 and 6.8 respectively. The immediately obvious difference between the EBIC images of type A and type B devices is in the ratio of the dark and light contrast over the total cell surface (compare Figs 6.4 and 6.8).As with type A devices increasing the accelerating voltage did not affect the general form of the EBIC contrast (Figs 6.9 and 6.10). Further, the characteristics of EBIC contrast for type A and type B devices persisted in both forward and reverse bias ($-400 < V_{bias} < +400$ mV), and with different angles of beam incidence. Comparison of the SE micrographs in Figs 6.3 and 6.7 with the EBIC micrographs in Figs 6.4 and 6.8 reveals that dark EBIC contrast appears preferentially at those places where kink sites and ledges are concentrated. Typical examples of this are marked at A, B, C on Figs 6.7 and 6.8 which are for type B devices. Dark contrast in an EBIC image implies a smaller EBIC current relative to that in a region of light contrast. If the effects of bombardment with an electron beam are assumed to be similar to those of an incident light beam, then the contrast observed in EBIC images would suggest that the photovoltaic efficiency of a dark contrast region is significantly smaller than that of a light contrast region. If the correlation between EBIC contrast and the consequent photovoltaic sensitivity of the local surface topography of CdS/Cu_2S cells is extended to the entire surface, it would be expected that the total area of active regions on type B devices would be far smaller than for type A cells.

To investigate this difference further the SEM was operated in the stationary spot mode and current voltage measurements were made on

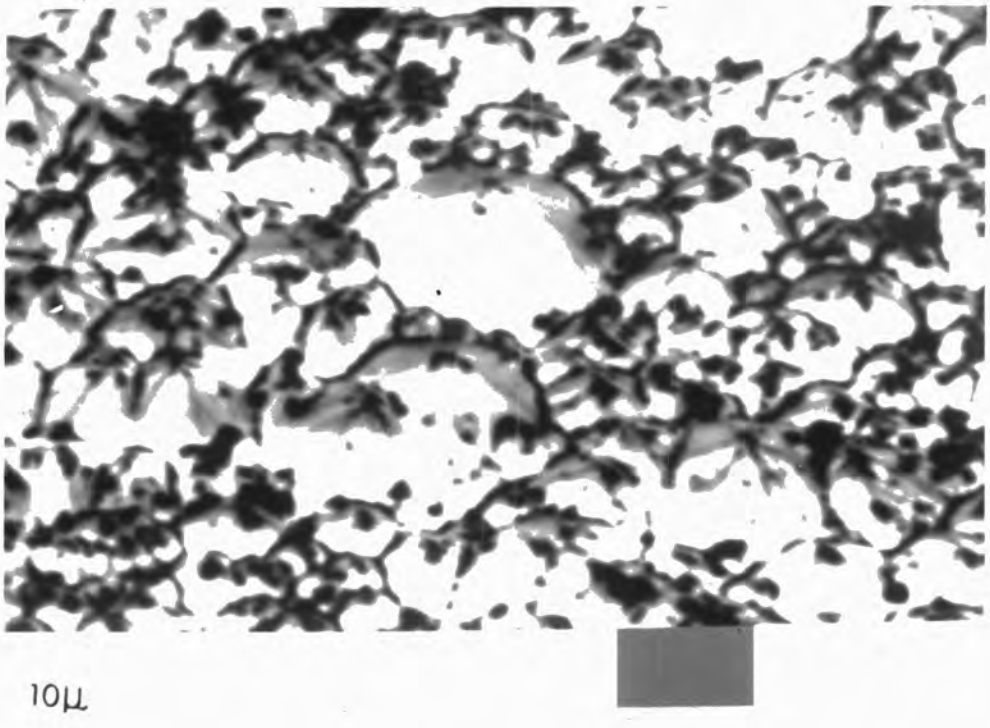


Figure 6.5 : EBIC Micrograph of another type A cell (at E_o = 7.5 keV) showing larger area of surface.

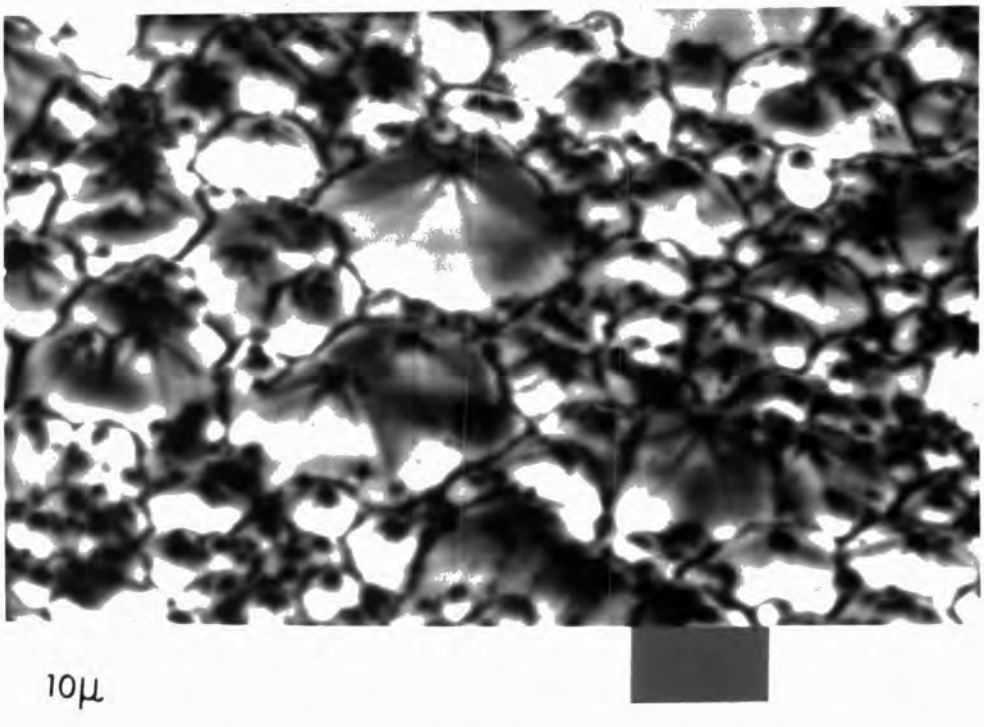


Figure 6.6 : EBIC Micrograph (at E_o = 25 keV) of region shown in Fig 6.5.

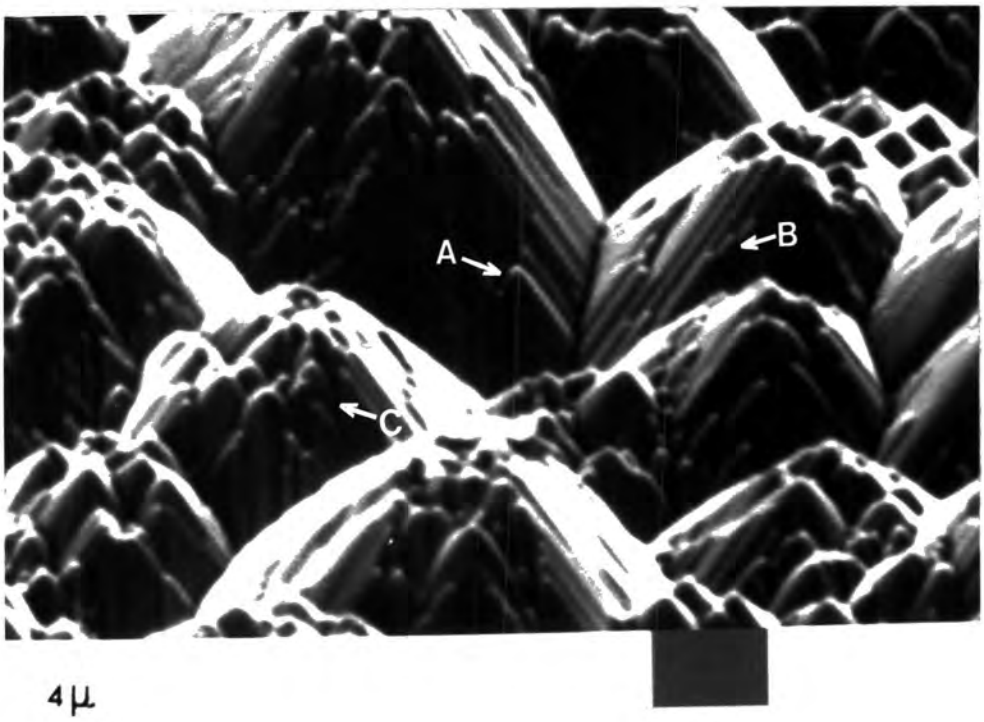


Figure 6.7 : Secondary Emission micrograph of a CdS/Cu_2S type B device surface.

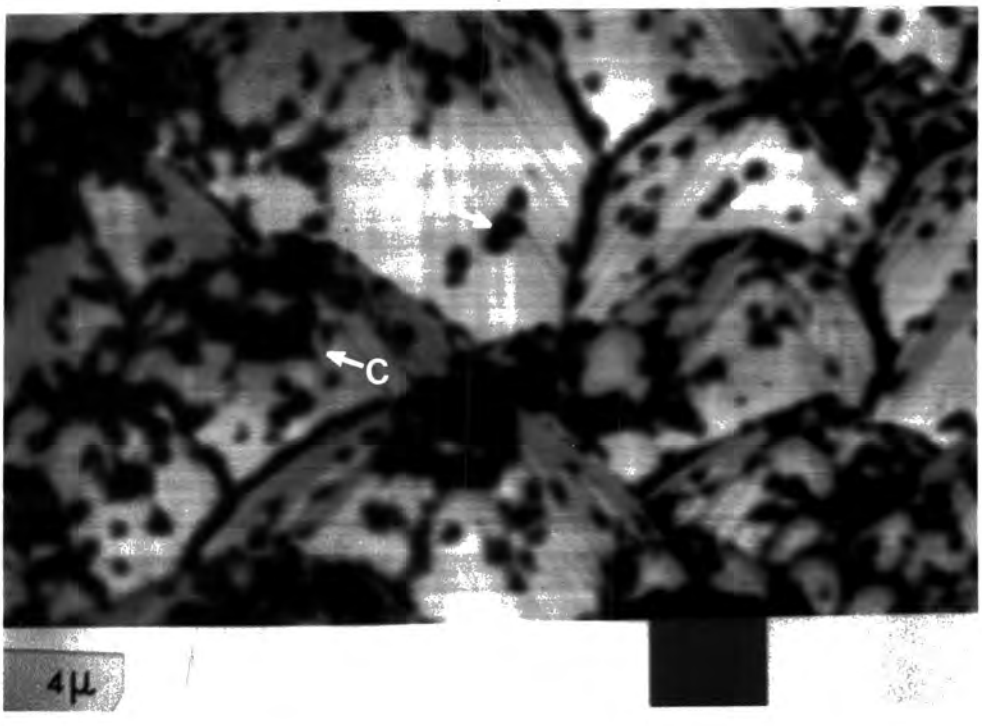


Figure 6.8 : Electron Beam Induced Current Image of the type B device shown in Fig 6.7 (E_o = 7.5 keV).

as-prepared type A and type B devices with the spot positioned first on a region of dark EBIC contrast then on one of bright contrast. Beam energies of 7.5 keV and 25 keV were used. Finally the I-V characteristics were recorded with the electron beam switched off. This gives the dark characteristics of the cells. Some results for type A and type B cells are shown in Figs 6.11 and 6.12. The comparison of these characteristics with those obtained under AM1 illumination (see Chapter 5, Figs 5.16 and 5.17) provides further confirmation of the similarities between an electron beam and optical excitation. Thus an electron beam can be used to probe the sensitivity of the cell to light. Although the values of V_{oc} obtained for as-prepared type A and B cells were quite close to those measured under AM1 illumination, J_{sc} values measured were very small because of the small irradiated area. All I-V characteristics were measured with the current amplifier set at fixed gain to be able to make direct comparison between curves measured with different beam energies and different samples. Thus the important features in comparing the I-V characteristics of type A and B devices (Figs 6.11 and 6.12) are :

(i) with a 25 keV beam: the value of I_{sc} when the beam was incident on areas of light contrast was larger than that with the beam incident on areas of dark contrast in both types of device, but the difference was most significant with type B devices. With type A cells V_{oc} was almost the same regardless of the beam position ; in contrast V_{oc} was twice as large when the beam was incident on light contrast regions in type B cells. The fill factors in type A cells were about three times larger than those in type B cells.

(ii) with a 7.5 keV beam : the differences in the values of I_{sc} with the beam incident on regions of light and dark contrast were not as large as they were with a 25 keV beam. This applied to both types of device. V_{oc} was slightly larger in type B cells when the beam was incident on the light EBIC contrasts and position independent with type A cells.

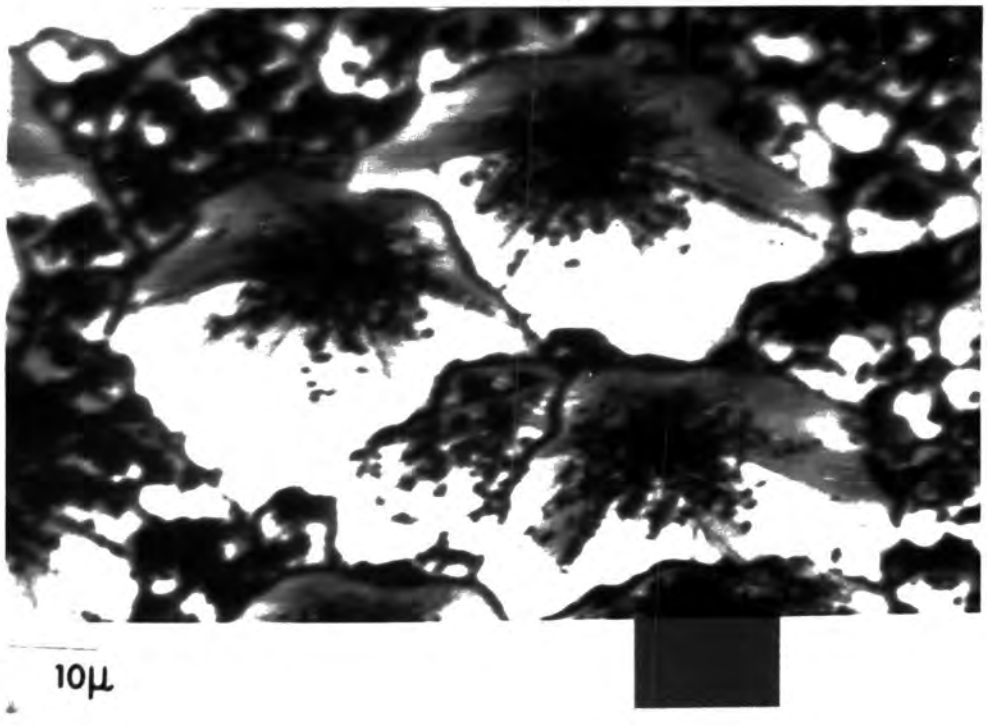


Figure 6.9 : EBIC Micrograph of another type B cell (at E_o = 7.5 keV) showing larger area of surface.

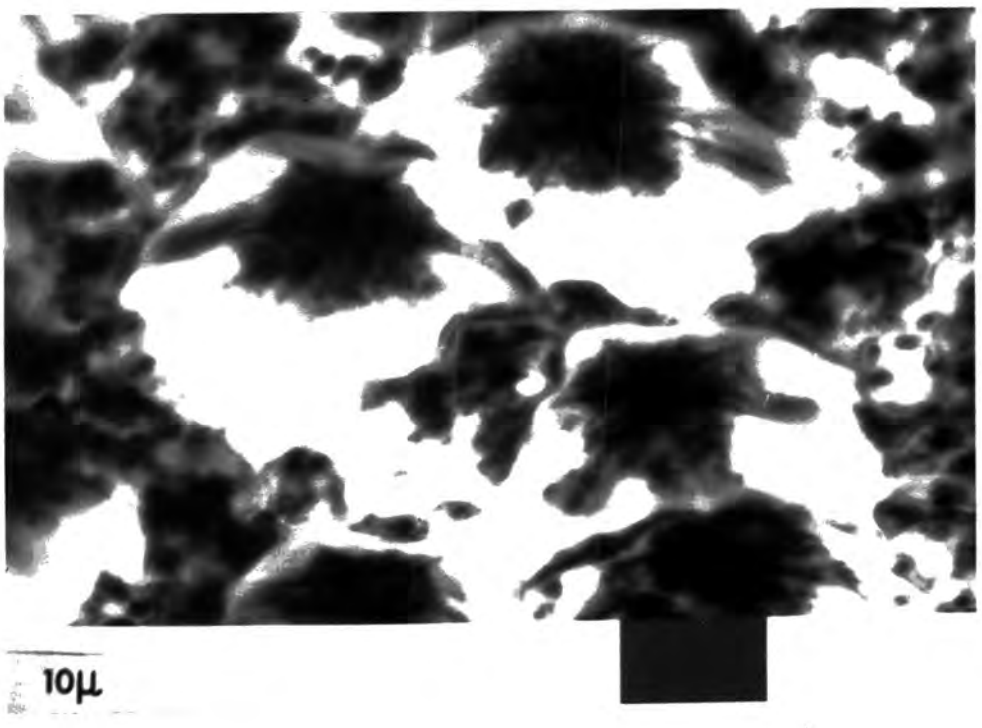
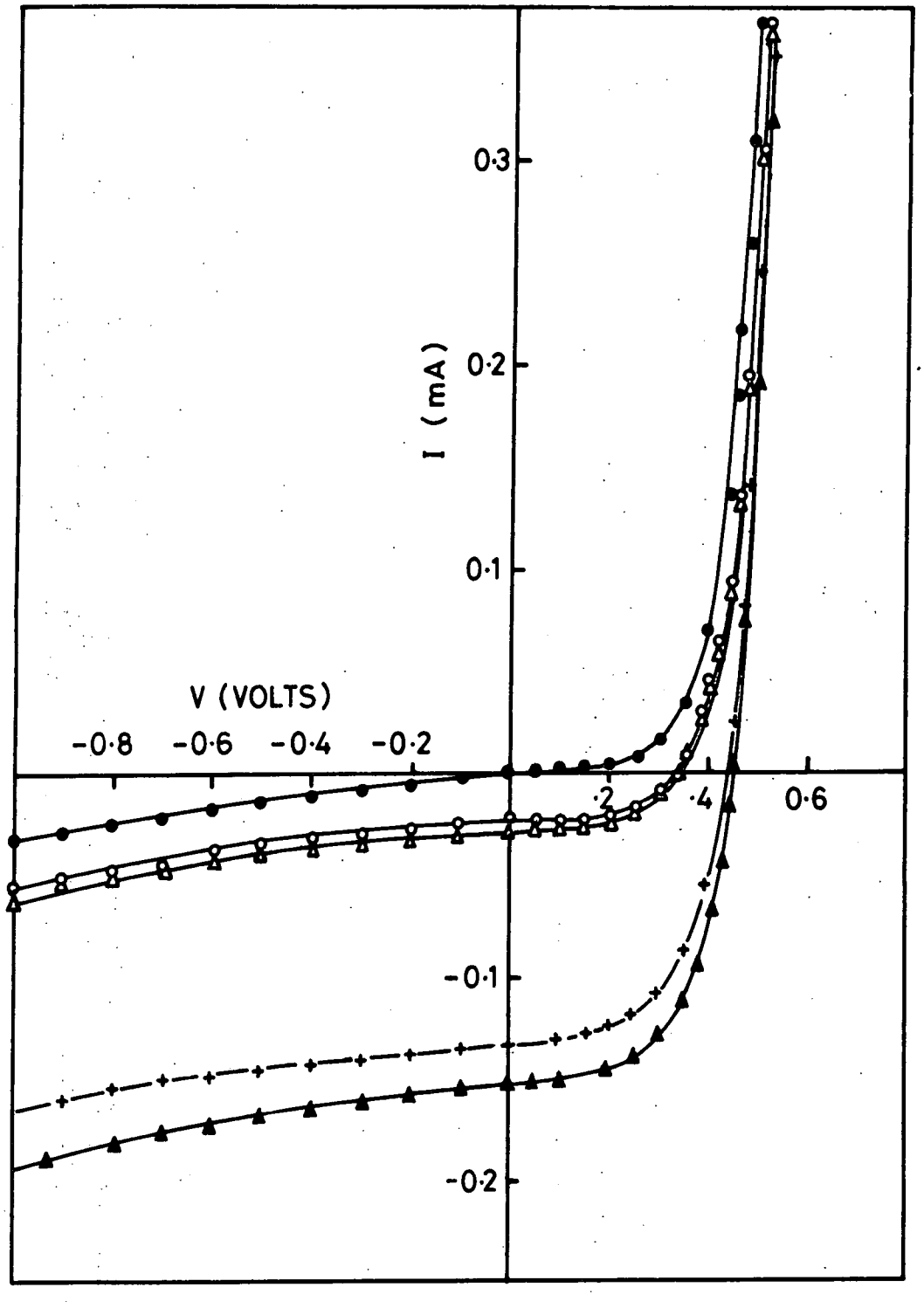


Figure 6 10 : EBIC Micrograph (at E_o = 25 keV) of region shown in Fig 6.9.



-●-●- in the dark

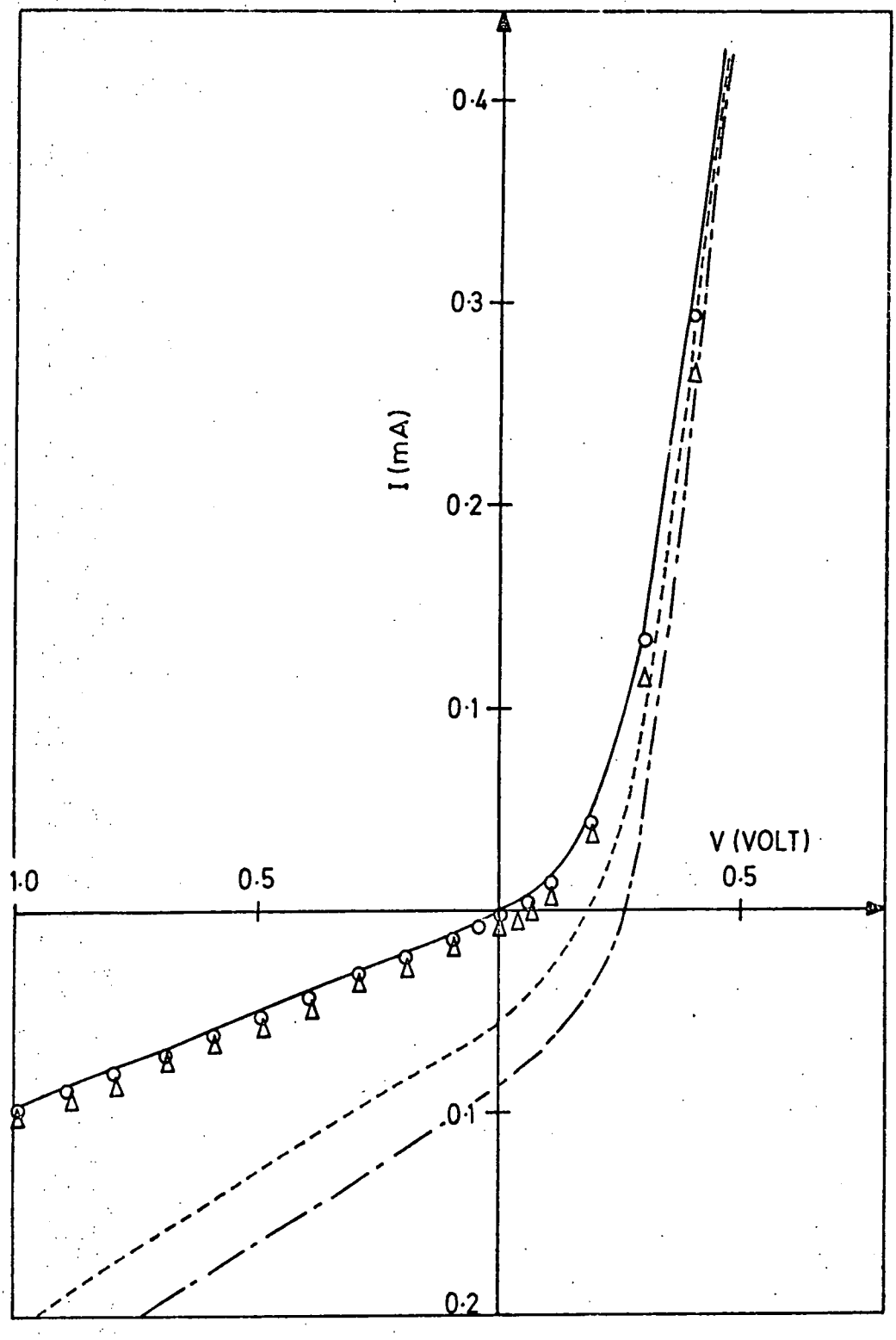
-o-o- with electrons of energy 7·5 Kev incident on dark EBIC contrast

-Δ-Δ- .. .. 7·5 Kev .. .. light .. ..

-+-+- .. .. 25 Kev .. .. dark .. ..

-▲-▲- .. .. 25 Kev .. .. light .. ..

FIG.6·11. CURRENT - VOLTAGE CHARACTERISTICS FOR AS-MADE TYPE A CELL IN THE DARK AND UNDER ELECTRON BEAM IRRADIATION



——— in the dark

oooo with electrons of energy 7·5 Kev incident on dark EBIC contrast

ΔΔΔΔ .. .. 7·5 Kev .. .. light .. ..

– – – – .. .. 25 Kev .. .. dark .. ..

—·— .. .. 25 Kev .. .. light .. ..

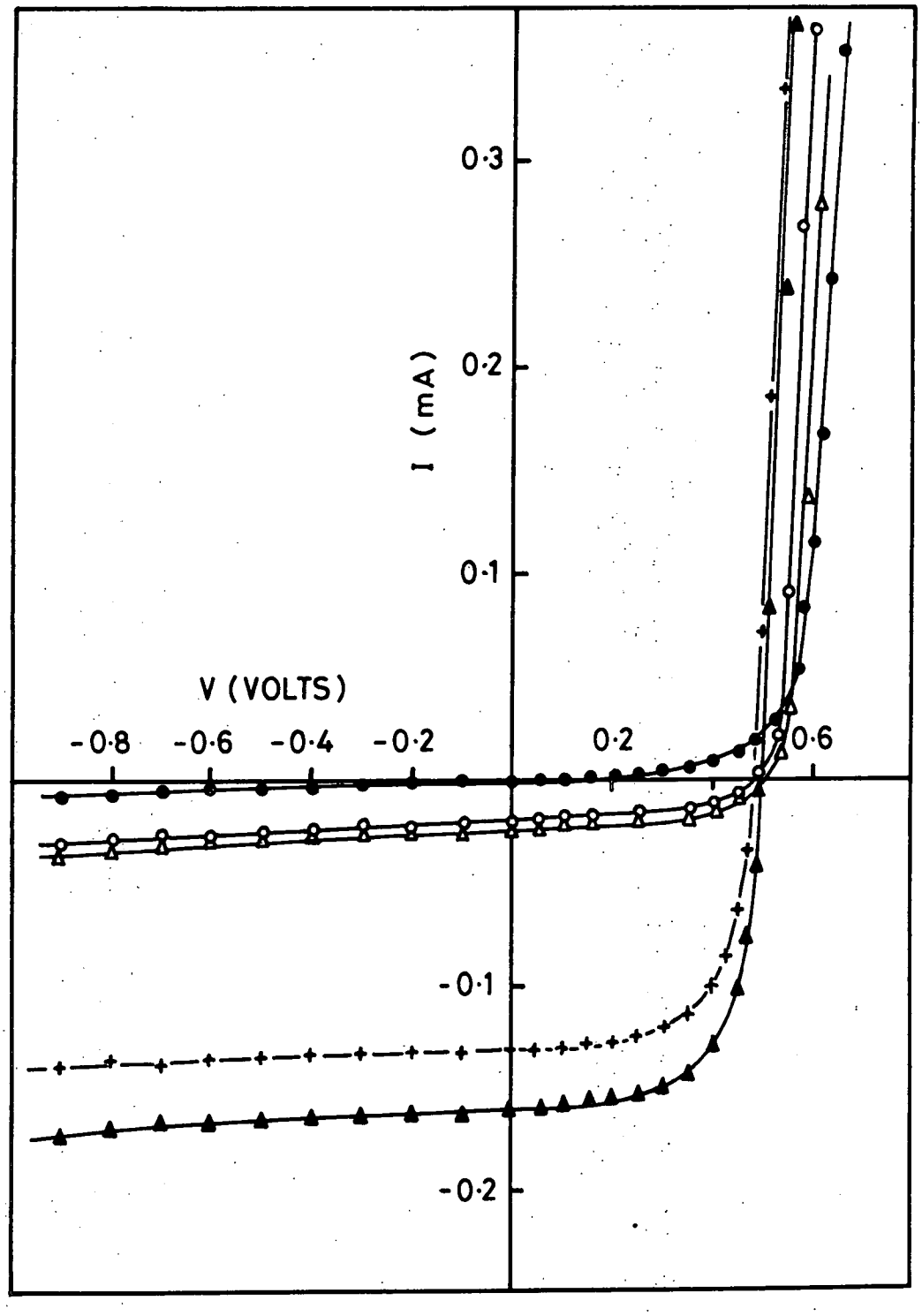
FIG.6·12.CURRENT - VOLTAGE CHARACTERISTICS FOR AS-MADE TYPE B CELL IN THE DARK AND UNDER ELECTRON BEAM IRRADIATION

(iii) the magnitudes of V_{oc} and I_{sc} in all cells increased significantly as the beam energy was increased from 7.5 keV to 25 keV with the beam on dark and light contrast regions but the improvement was larger for type A cells.

(iv) dark I-V characteristics and characteristics measured with different beam energies converged towards each other in forward bias but did not cross over.

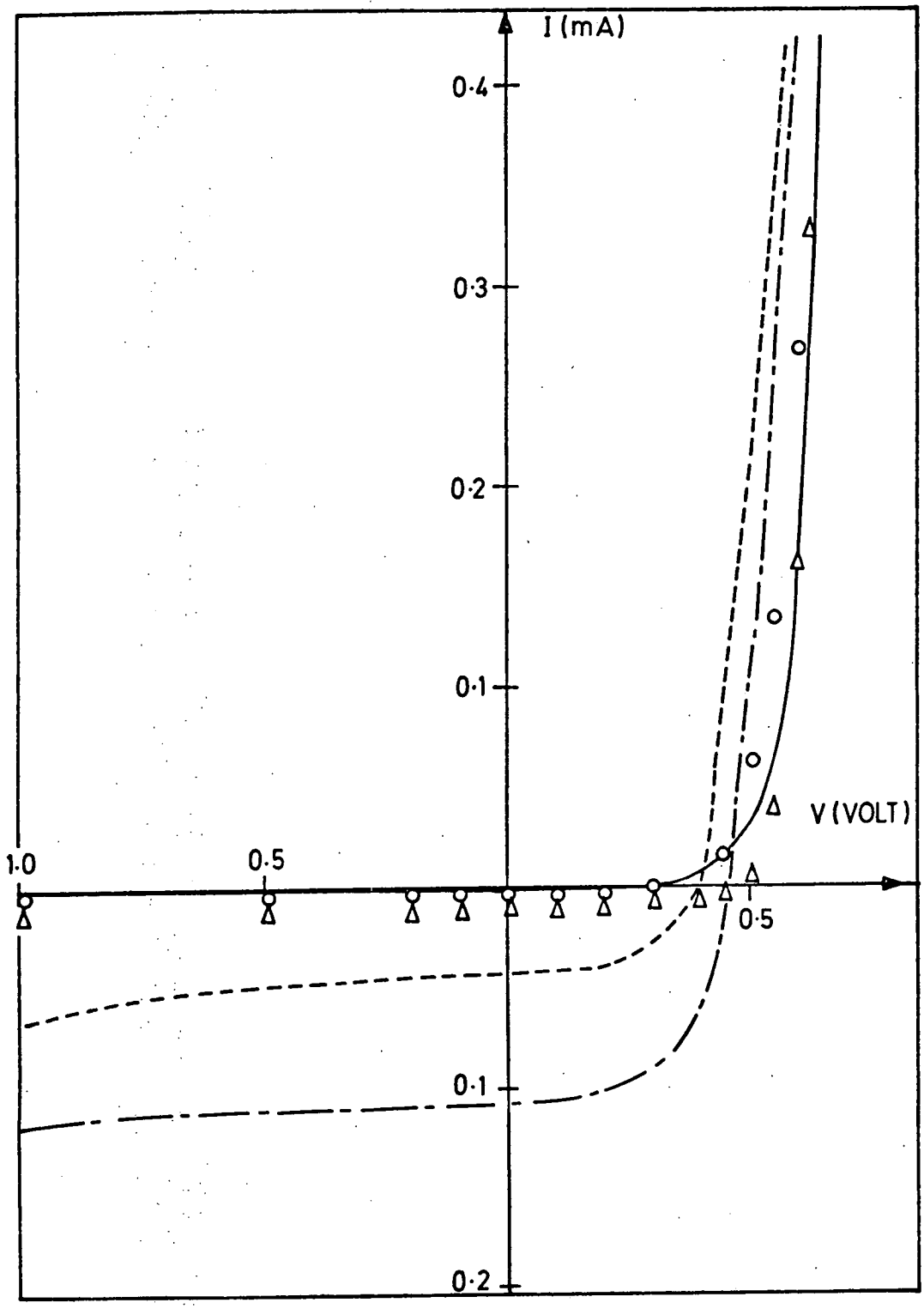
6.4 EFFECT OF A POST BARRIER AIR-BAKE ON EBIC CONTRAST AND PHOTOVOLTAIC SENSITIVITY

After the EBIC study of the as-prepared cells had been completed a two minute post barrier air-bake at 200°C was administered to all samples and the EBIC study of them carried out again. The general features of the contrast were essentially unchanged. However, the current voltage characteristics measured with the beam on the regions of opposite contrast after an air-bake are presented in Fig 6.13 and Fig 6.14 respectively. The important features are : (1) the heat treatment of type A devices had a slightly beneficial effect in that the dark reverse current was reduced while the fill factor was increased by a small amount (2) with a 25 keV beam (a) I_{sc} for the beam incident on a region of light contrast increased slightly (from 0.15 mA to 0.16 mA) but for the beam incident on a region of dark contrast it remained unchanged, (b) V_{oc} values showed little increase when regions of either contrast were bombarded (3) when the beam energy was reduced to 7.5 keV, the I_{sc} values exhibited a drastic decrease for both types of contrast and the difference between the values of I_{sc} for the beam incident on regions of opposite contrast became very small (4) V_{oc} values measured were almost independent of the energy and the position of the beam. The post barrier air-bake also introduced a cross over effect so that the characteristics in the dark and under bombardment crossed over one another at forward biases between 0.4 and 0.5V. Similar effects were



-●-●- in the dark
-o-o- with electrons of energy 7·5 Kev incident on dark EBIC contrast
-Δ-Δ- .. .. 7·5 Kev .. .. light .. ..
-+-+- .. .. 25 Kev .. .. dark .. ..
-▲-▲- .. .. 25 Kev .. .. light .. ..

FIG.6·13. CURRENT - VOLTAGE CHARACTERISTICS FOR TYPE A CELL , AIR-BAKED AT 200°C FOR 2 MINS , MEASURED IN THE DARK AND UNDER ELECTRON BEAM IRRADIATION



——— in the dark

oooo with electrons of energy 7·5 Kev incident on dark EBIC contrast

ΔΔΔΔ .. .. 7·5 Kev .. .. light .. ..

– – – – .. .. 25 Kev .. .. dark .. ..

—·— .. .. 25 Kev .. .. light .. ..

FIG.6·14. CURRENT - VOLTAGE CHARACTERISTICS FOR TYPE B CELL, AIR-BAKED AT 200 C FOR 2 MINS, MEASURED IN THE DARK AND UNDER ELECTRON BEAM IRRADIATION

observed when the whole surface area was irradiated with AM1 radiation (see Chapter 5).

A post barrier air-bake was essential to improve the shape of the characteristic and the performance of type B cells (see Chapter 5). However, after heat treatment, the I_{sc} values showed more diversity between areas of different contrast. The values of V_{oc} increased noticeably when both areas were bombarded, but the region of light contrast always yielded the larger open circuit voltage, (see Fig 6.14 for a graphical representation of the results).

6.5 MEASUREMENTS OF MINORITY CARRIER DIFFUSION LENGTHS

The mean distance a minority carrier travels in a semiconductor before being lost through recombination is called the diffusion length, L. Since the efficiency of photovoltaic devices is very sensitive to the magnitude of L, it is important to be able to measure its value accurately. The measurement however is a difficult one and while many techniques have been employed, there is still a serious lack of agreement among the values obtained by the various methods.

In this investigation, the EBIC current collected at the junction was measured as a function of beam distance from the junction on both sides. The simplified schematic experimental arrangement is shown in Fig 6.2. For the geometry involved, the incident electron beam is scanned along a line perpendicular to the p-n junction over a cleaved surface normal to the junction plane.

The calculation of the variation of the EBIC current with the distance, x, of the beam from the junction was first done by Kyser and Wittry[15]. Assuming that there is no electric field in the material except at the junction, the minority carrier density obeys the diffusion and continuity equations and in terms of the excess carrier concentration, $\delta n_p = n_p - n_o$ in p-type material, where n_p and n_o are the non-equilibrium

and equilibrium electron concentrations respectively. It follows that ;

$$D_n \nabla^2(\delta n_p) - \frac{\delta n_p}{\tau} + G_T = 0 \qquad (6.4)$$

where D_n is the minority carrier (electron) diffusion coefficient and τ_n is the minority carrier lifetime. Re-arranging Eq.(6.4) and substituting $L_n^2 = D_n \tau_n$, the equation can be re-written as

$$\nabla^2(\delta n_p) - \frac{\delta n_p}{L_n^2} = - \frac{G_T}{D_n} \qquad (6.5)$$

A similar equation applies for excess holes in n-type material. If the electron beam is assumed to be a point source with a generation volume having spherical symmetry, the appropriate solution of Eq.(6.5) will be

$$\delta n = \gamma \, e^{-r/L} \Big/ r \qquad (6.6)$$

where γ is a constant with dimensions cm^{-2}. The number of minority carriers that reach the junction and are therefore collected is given by the value of $- D \frac{\partial \delta n}{\partial x}$, at the junction ($x = 0$) integrated over the plane of junction. Thus the EBIC current is given by

$$I(x) = 2\pi \gamma D \, e^{-x/L} \qquad (6.7)$$

where $2\pi\gamma D$ directly depends on the strength of the source and is equal to $I(o)$ when all surface and interface effects are negligible. Hence, in the simplest one dimensional case, the short circuit EBIC collected by a planar junction will be of the form

$$I(x) = I(o) \exp\left(-\frac{x}{L}\right) \qquad (6.8)$$

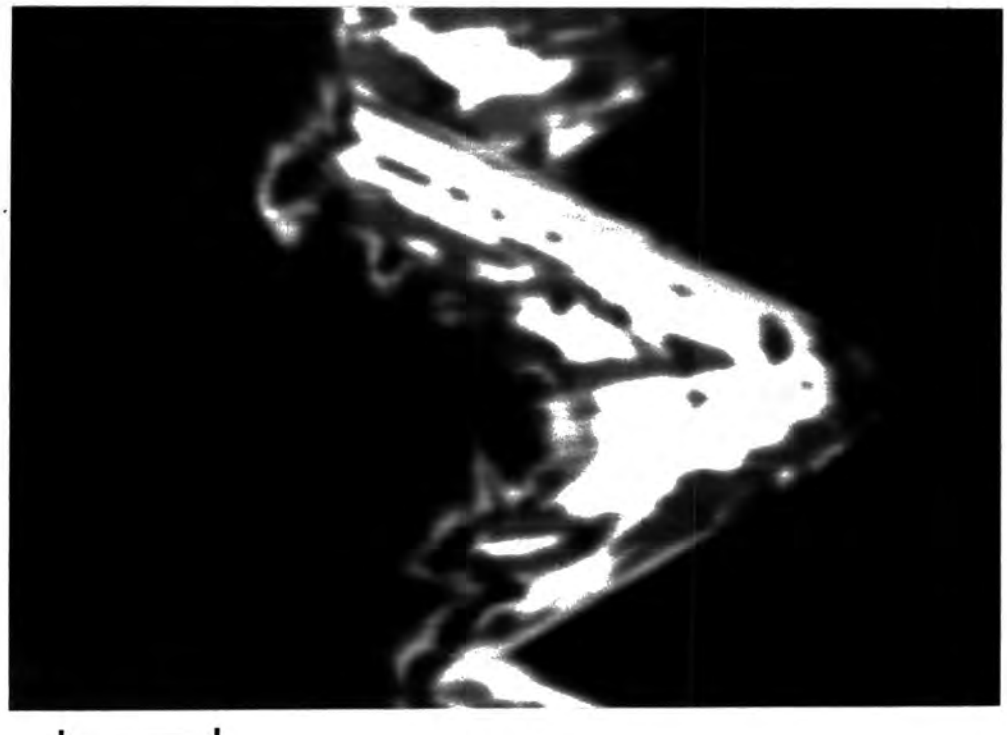
6.5.1 Minority Carrier Diffusion Lengths in As-Prepared Samples

In an attempt to measure diffusion lengths y-modulated line scans

were made across junctions which had been exposed by cleaving in a direction normal to the junction plane. Figs 6.15 (a-b) demonstrate the secondary emission (SE) and EBIC micrographs for part of the junction of a cleaved device which was prepared by plating the sulphur face in the standard solution for 10s. However, as these figures show the junctions cannot be precisely defined and are unsuitable for diffusion length measurements. In order to reduce the surface effects and to define the junction more clearly devices were prepared with much thicker layers of copper sulphide. Figs 6.16 (a) and (b) show the SE and EBIC micrographs of the junction of a sample plated for 30s. The thickness of copper sulphide was about 1.5 μm. All the measurements of minority carrier diffusion lengths were made with beam energies of 7.5 kV to avoid the errors introduced by using a large generation volume. Fig. 6.17 shows a typical line scan across the junction. Assuming that equation 6.8 is valid, diffusion lengths have been calculated from the slope of a plot of $\log\frac{I(x)}{I_o}$ versus x. In Fig. 6.19 open circles represent data from an as-prepared cell with L_n = 0.26 μm in Cu_xS and L_p = 1.09 μm in the CdS. Calculated values of diffusion lengths from the two sides of devices prepared under different conditions are listed in Table 6.1. Measurements made from a number of traces taken on the same sample show that there is a significant variation in the short circuit current along the junction, however measured diffusion lengths agreed within the sensitivity of experiment. Further, it has been found that the diffusion lengths measured did not show any significant variation with samples carrying different phases of Cu_xS. The diffusion lengths in Cu_2S differ from each other by less than 0.05 μm at the most. In contrast, the values of L_p measured on the CdS side of as-made devices showed a considerable spread ($0.364\ \mu m \leq L_p \leq 1.09\ \mu m$).

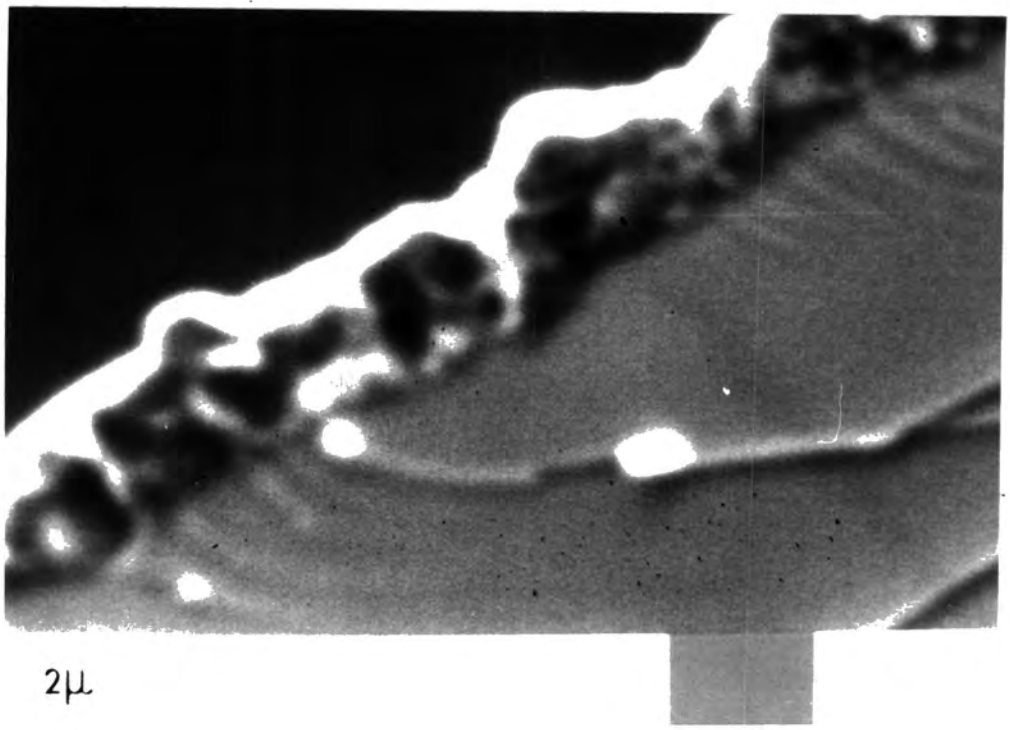
Although data obtained from the line scans match with the exponential decaying model discussed in the previous section, the shape of the maxima of the semi-log plots of EBIC current against distance show significant

(a)

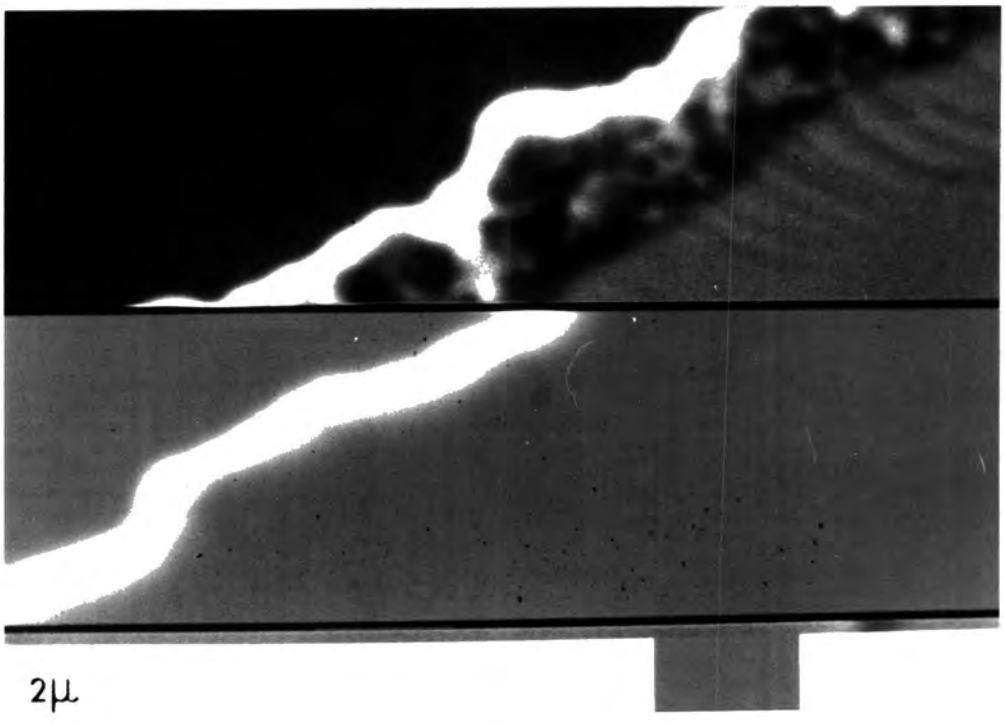


(b)

Figure 6.15 : Cleaved Cross-Section of CdS/Cu_2S cell chemiplated for 10s.
(a) secondary emission micrograph, (b) EBIC image (at E_o = 7.5 keV).



(a)



(b)

Figure 6.16 : Cleaved Cross-Section of CdS/Cu_2S cell chemiplated for 30s. (a) secondary emission micrograph (b) mixed (SE + EBIC) image (E_o = 7.5 keV).

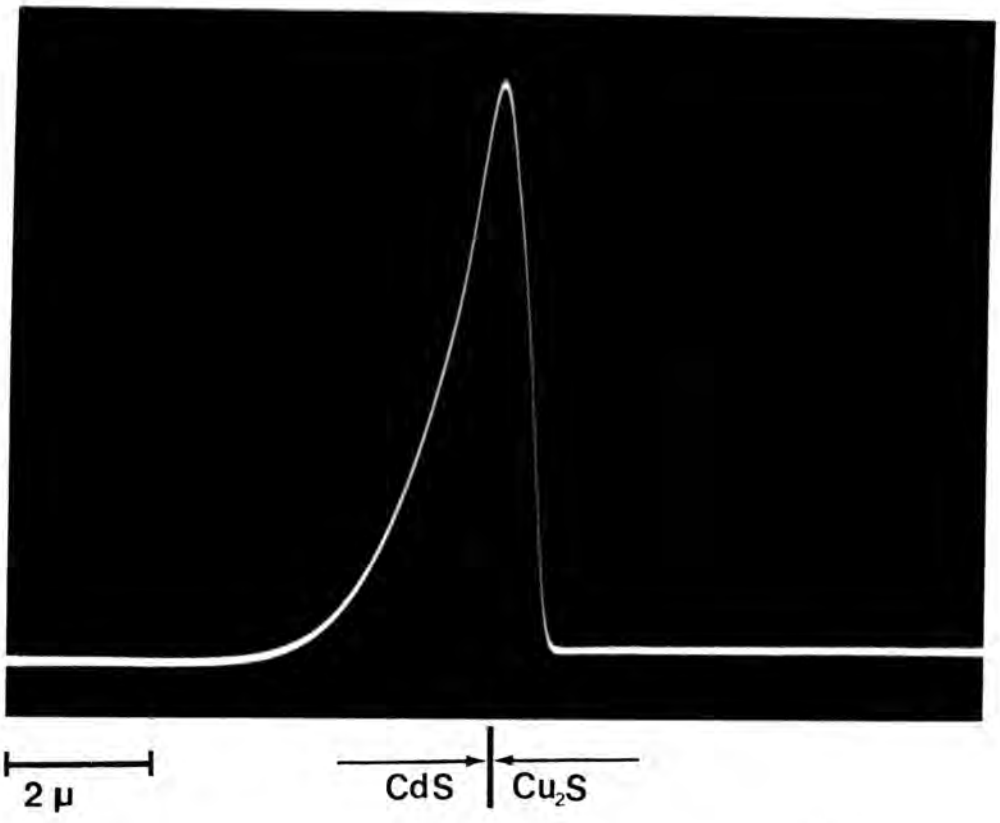


Figure 6.17 : EBIC single line trace across the junction of an as-made CdS/Cu_2S heterojunction

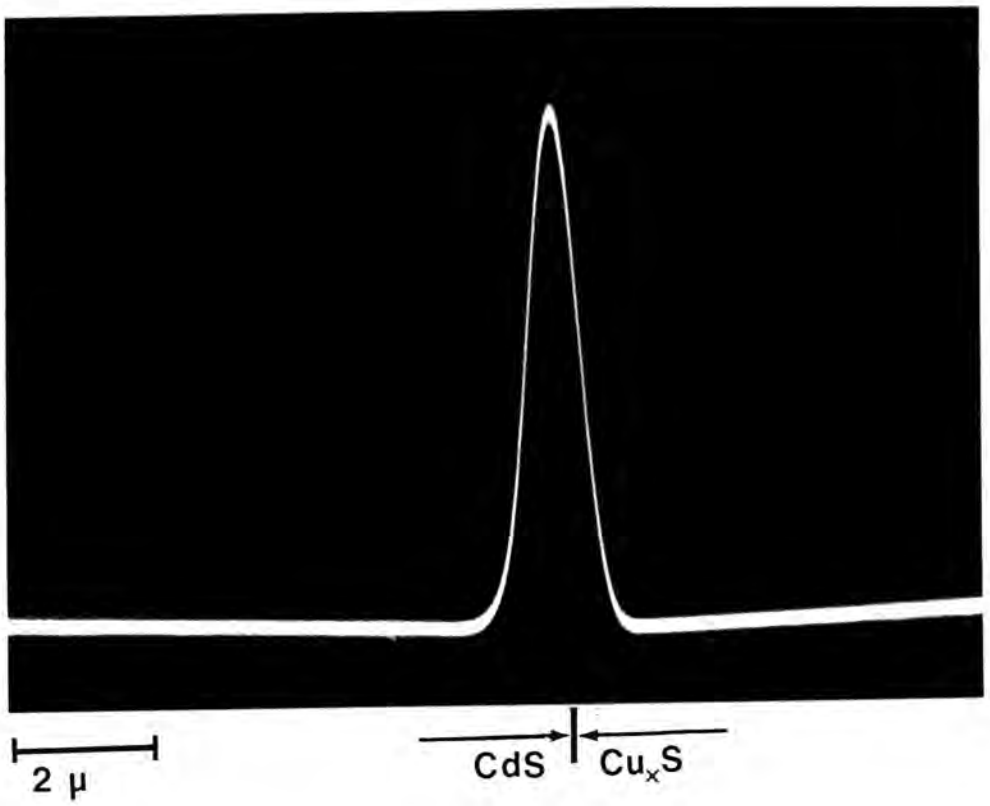


Figure 6.18 : EBIC single line trace across the same junction as in Fig 6.17 after a 2 minute air-bake

PREPARATION DETAIL	Minority Carrier (Hole) Diffusion Length in CdS				Minority Carrier (Electron) Diffusion Length in Cu_xS			
	As-Made		Air-Baked for 2 mins at 200°C		As-Made		Air-Baked for 2 mins at 200°C	
	L_p (μm)	Correlation Coefficient	L_p (μm)	Correlation Coefficient	L_n (μm)	Correlation Coefficient	L_n (μm)	Correlation Coefficient
Etch for 30s and	0.385	0.996	0.298	0.995	0.239	0.993	0.225	0.998
Dipped for 30s.	0.405	0.998	0.281	0.993	0.241	0.997	0.223	0.991
Etch for 30s and	0.364	0.989	0.286	0.997	0.225	0.988	0.235	0.990
Dipped for 1 min.	0.380	0.989	0.300	0.993	0.232	0.989	0.265	0.989
Polished with 1 μm Al_2O_3	0.764	0.994	0.380	0.992	0.215	0.987	0.255	0.988
and Dipped for 30s.	1.04	0.997	0.356	0.998	0.245	0.976	0.272	0.981
Polished with 1 μm Al_2O_3	0.425	0.978	0.295	0.985	0.243	0.968	0.230	0.978
and Dipped for 1 min.	0.402	0.989	0.260	0.995	0.232	0.966	0.220	0.986

TABLE 6.1 : Minority carrier diffusion lengths in the CdS and Cu_xS before and after a post barrier air-bake (the values for the same sample measured from different line traces).

variations from sample to sample. Comparison of Fig 6.19 and Fig 6.20 demonstrates this clearly. In Fig 6.19 the deviation from linearity below 0.2 μm on the CdS side and the broadened peak suggest that a depletion region of about the same width exists. In contrast one of the plots in Fig 6.20 shows a sharp peak at the junction indicating a narrow depletion region (∿ 0.1 μm). However, this could be a consequence of different deep donor concentrations. Fig 6.21 has two different slopes on the CdS side of the junction. This may indicate that the minority carrier had different diffusion lengths in two adjacent regions.

6.5.2 Minority Carrier Diffusion Lengths After Post Barrier Air-Bake

After the measurements had been completed on the as-prepared cells, the devices were given a heat treatment at 200°C for 2 minutes. Then in order to avoid the effects of possible oxidation of the exposed cross-sections of junctions cleaved prior to the bake, the cells were cleaved again in the same direction. In this way measurements were made on a freshly exposed cross-section of Cu_xS and CdS. EBIC current-distance curves for heat treated cells are plotted semi-logarithmically in Figures 6.19, 20 and 21 (triangles). Calculated values of diffusion length in Cu_xS and CdS following a post barrier air-bake are also listed in Table 6.1. The measured values of L_n on the Cu_xS side did not change significantly but the L_p values on the CdS side decreased considerably.

6.6 DISCUSSION AND CONCLUSION

(i) EBIC Image Contrast and Local Sensitivity

In order to understand the possible origin of the contrast in EBIC images and the corresponding current transport mechanisms, several parameters have to be considered. One of the most important effects is the interaction of the electron beam with CdS and Cu_xS. Using equation 6.2 the ranges of 7.5 keV and 25 keV electrons are calculated to be R_G (7.5 keV) =0.392 μm and R_G (25 keV) = 4.61 μm in Cu_xS and R_G (7.5 keV) =0.549 μm and R_G(25 keV)= 6.45 μm in CdS. The effective depth of penetration is half of these values[12,13].

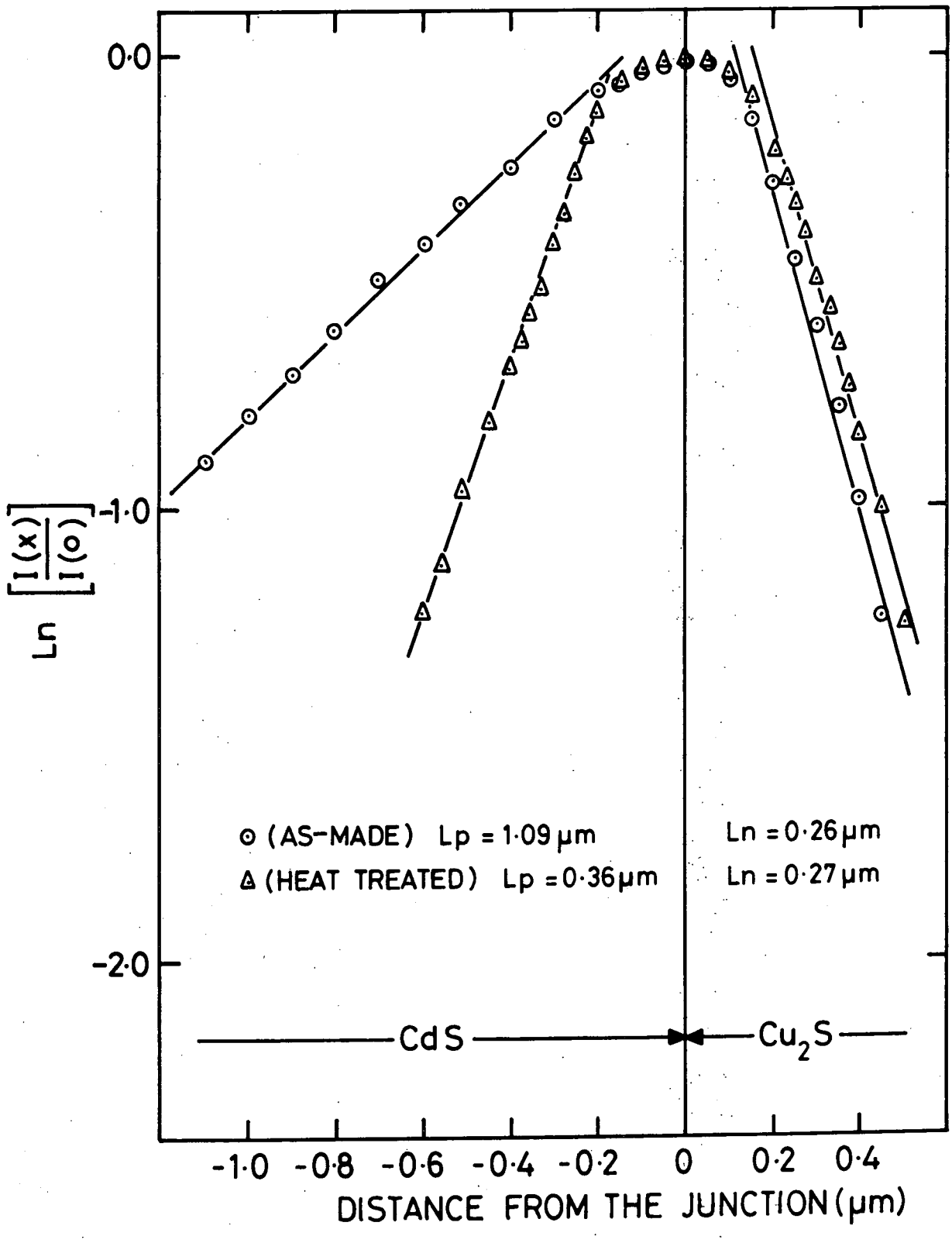


FIG. 6·19 SEMI-LOG PLOT OF THE RELATIVE EBIC CURRENT VERSUS CURRENT FROM THE JUNCTION, (⊙) AS-MADE (Δ) AFTER 2 mins. HEAT TREATMENT IN AIR AT 200°C

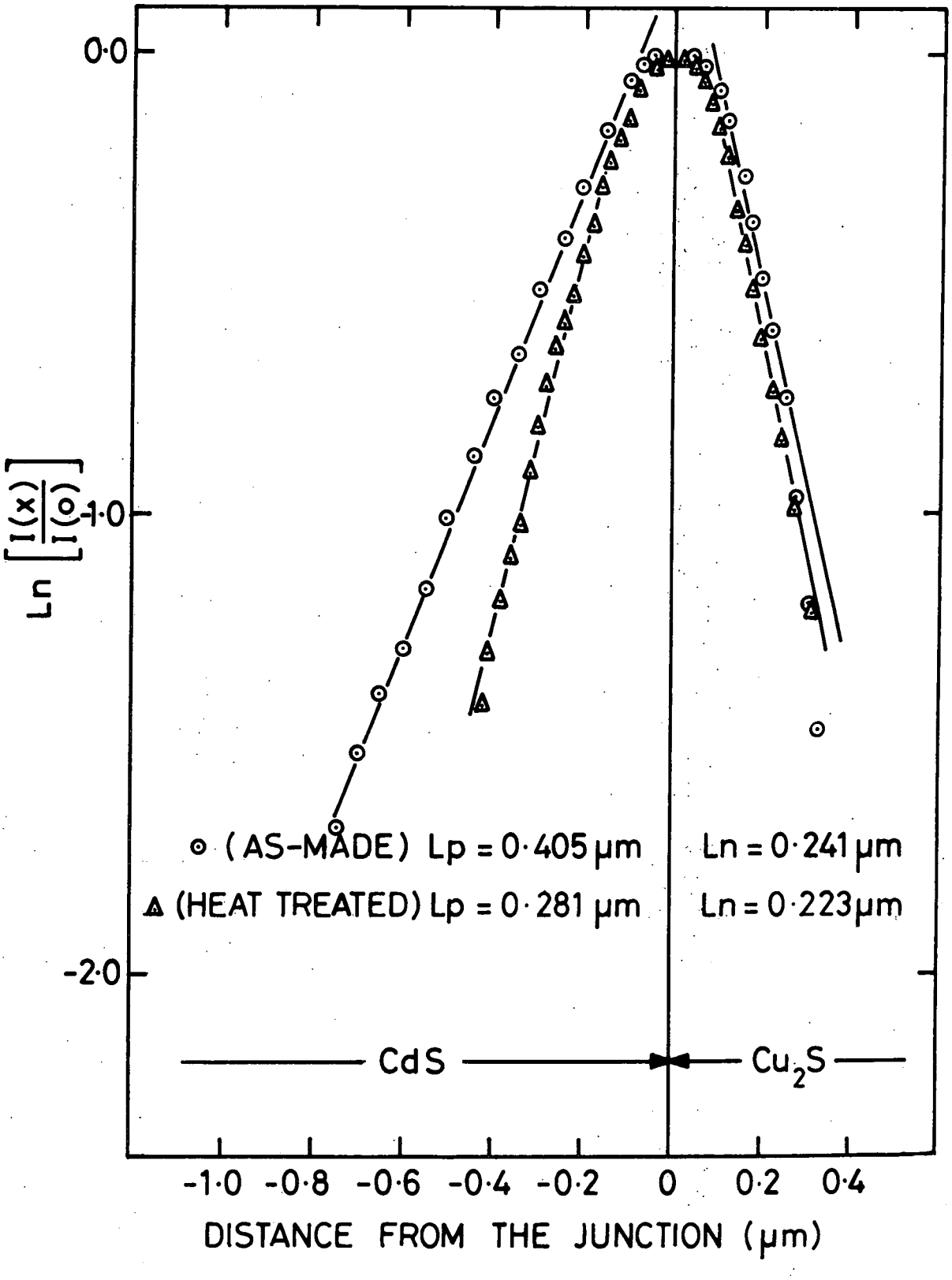


FIG. 6·20 SEMI - LOG PLOT OF THE RELATIVE EBIC CURRENT VERSUS DISTANCE FROM THE JUNCTION
(⊙) AS-MADE (△) AFTER 2mins. HEAT TREATMENT

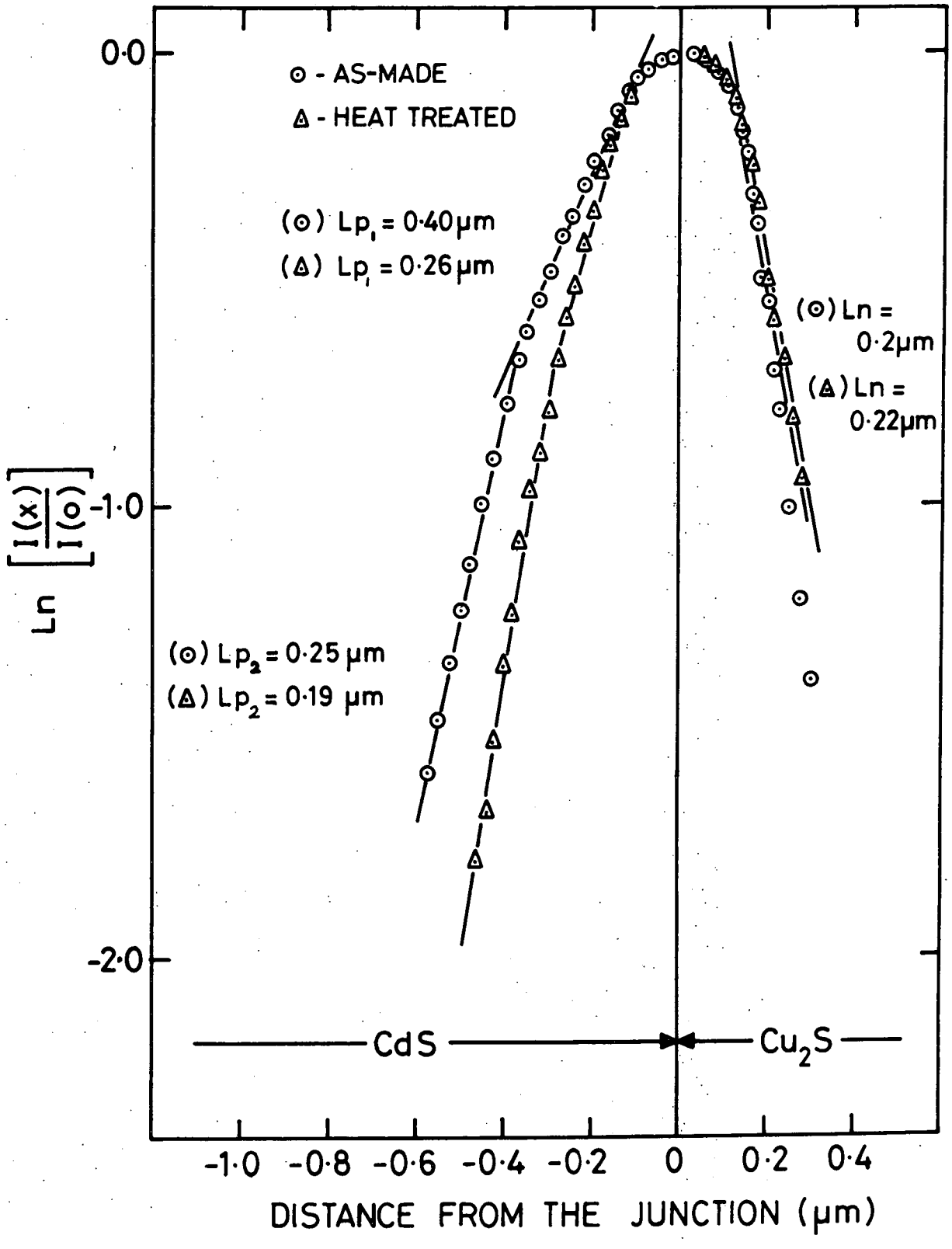


FIG. 6·21 SEMI-LOG PLOT OF THE RELATIVE EBIC CURRENT VERSUS DISTANCE FROM THE JUNCTION
(⊙) AS-MADE (Δ) AFTER 2mins. HEAT TREATMENT

Since the thickness of the copper sulphide layer in the devices studied for EBIC contrast (10s dip) was about $\sim$ 0.25 μm (see Chapter 5, section 5.3.2) the effective depths of penetration at 7.5 keV was comparable to the thickness of the copper sulphide layer and most of the beam energy would be dissipated in Cu_xS. The generation rate in CdS is half of that in Cu_xS because of its higher bandgap, i.e. radiation, ionisation energies are 7.2 eV for CdS and 3.6 eV for Cu_2S[13]. It follows therefore that when a 7.5 keV electron beam scans the device surface parallel to the junction plane, the main contribution to EBIC current comes from the electrons generated in Cu_xS. On the other hand if a 25 keV electron beam impinges on the device a considerable number of electron-hole pairs will be generated in the depletion region and in the bulk of CdS. The net contribution to the EBIC current due to both generated electrons in the Cu_xS and holes in the CdS is limited by the minority carrier diffusion lengths in both materials. The measured minority carrier diffusion length in Cu_xS is about $\sim$ 0.2 μm which implies that only those electrons generated in Cu_xS within $\sim$ 0.2 μm region of the junction can reach the interface. As for the CdS side of the heterojunction the measured diffusion lengths showed a wide variation depending on device preparation and post-barrier treatments. (We return to this later). However, it is obvious that only those holes produced within a diffusion length have a chance of being collected. Referring to the band energy model shown in Chapter 3, section 3.4.2 (Fig 3.2) for heterojunctions, the conduction and valence band discontinuities ΔE_c and ΔE_v are due to the difference in the electron affinities and band gaps of the two materials, and a high density of interface states exists at the junction interface (for details see Chapter 3, section 3.3). Firstly, if we consider the electron-hole pairs generated in the Cu_xS, the minority carriers may recombine in the bulk or at the surface through interface states in which case the contribution to an induced current in an external circuit is zero.

However, electrons reaching the interface may be swept by the junction field into the bulk of the CdS. These electrons will either reach the back contact or recombine with holes supplied by the back contact : in both cases they will produce an EBIC current. A detailed discussion of the relation between the number of electrons which reach the interface and number which are collected is given in Chapter 3, section 3.7, where the interface collection efficiency is defined. The interface collection efficiency is a function of the electric field at the junction, F, the interface recombination velocity, S_I and the mobility (see Chapter 3). With the electron hole pairs created in the depletion region of CdS, holes will be accelerated towards the junction interface by the field, whereas electrons will be swept away from the interface. With a high electric field and a small density of interface states and Cu acceptors in the depletion region, recombination of created pairs can be small. However, the existence of a very high density of interface states at the junction and Cu acceptor centres in the depletion region alters the effective field, so that recombination of carriers in the depletion region and reduction of current becomes more significant.

The current loss can also be due to recombination at the free surface of the Cu_xS which depends on the thickness of the copper sulphide layer and the surface recombination velocity.

In our observations a realistic comparison of regions of different contrasts may only be made within the same micrograph and not between one micrograph and another because of the different DC offset used in the amplifier circuit to which the EBIC signal was fed. A dark contrast region represents a smaller current collection compared with light contrast regions. The copper sulphide layers were found to be thicker at the summits of the hillocks. One possibility therefore is that with a beam energy of 7.5 keV generation occurs outside the diffusion distance at the top of hillocks

so that these regions appear dark. However,the fact that the relative contrast did not change significantly when the beam energy was increased from 7.5 keV to 25 keV suggests that differences in thickness were not the determining factor. Comparison of Fig 6.5 and 6.6 for type A devices and of Fig 6.9 and 6.10 for type B devices demonstrates this elegantly. The most important difference between these micrographs is that much more detail was observed when the lower beam eneryg was used. This can be attributed to the comparable thickness of the copper sulphide layer and the effective depth of the generation volume at 7.5 keV beam energy. In this way the contribution of carriers generated in the CdS can be eliminated. We conclude that the origin of the EBIC image contrast was not strongly associated with variations in the thickness of the Cu_xS over the hillocks. The SE micrographs of type A devices indicate that ledges are more numerous near the tops of the hillocks, where the dark contrast appears preferentially. With type B devices careful comparison of the SE micrograph (Fig 6.7) and the EBIC micrograph (Fig. 6.8) demonstrates the important correlation between ledges or kink sites and the deliniation of EBIC contrast. Typical examples of this are marked A , B , C (see Fig 6.7 and 6.8). It appears therefore that the growth of Cu_xS on CdS is complicated in the presence of ledges and kinks, resulting in poorer junction properties at these sites. Evidently smooth surfaces are required if microscopically uniformly sensitive junctions are to be produced by the plating process. This conclusion is in a good agreement with that drawn in Chapter 5 from the strong correlation between the surface features and the ultimate behaviour of as-prepared cells.

The extent to which the junction was poorer at the dark regions corresponding to ledges and kink sites is indicated by the current-voltage characteristics shown in Figs 6.11 and 6.12 for type A and B cells in the as-prepared condition. The low current level in these devices is a consequence of irradiating a small selected area of the junction with a

stationary beam with a spot diameter $\sim$ 0.03 μm.

The good diode characteristics and high performance as solar cells of type A devices, and the poor characteristics and low performance of type B devices in the as-made condition can now be explained. The existence of more numerous surface steps and kink sites results in a very complex interface between Cu_xS and CdS in such regions. It is likely that the density of interface states will be higher there. Higher interface state densities give rise to current flow via tunnelling recombination paths at low activation energies (see section 3.7.1) and local variations in the density of interface states lead to large local variations in the diode behaviour. For instance, Fig 6.12 represents the total behaviour of a type B device, but the differences in I_{sc} and V_{oc} with the beam positioned on the light EBIC contrast and dark EBIC contrast reveal that locally the junction behaves quite differently in these regions. In type A devices this difference exists between the very top of a hillock and its sloping side (which are dark and light in EBIC contrast respectively). Although this variation in EBIC current might be attributed to the different angles of beam entrance, at the top and sloping sides of a hillock, examination of I_{sc} and V_{oc} when the electron beam was incident on closely spaced regions of different contrast showed that the effects of different entry angle can be disregarded. The power conversion efficiency was twice as large when the beam was incident on the light EBIC contrast than when it was incident on a region of dark contrast. The conclusion is therefore that the photovoltaic efficiency probably varies over the surface in the same way, so that a large increase in the rectifying behaviour of the diode and the efficiency of the cell would be expected if substrates with regular and smooth surfaced hillocks were employed.

The role of an air-bake at 200°C on type A devices and type B devices has been discussed in detail in Chapter 5. In fact the change in shape of the characteristics following the air-bake for both types of device can be explained in terms of the production of a photoconductive compensated layer

in the CdS by copper migration. The effect of this layer on the device characteristics has also been discussed in Chapter 5. The forward characteristic in Fig 6.14 measured for an incident beam energy of 25 keV has a larger slope than the curve measured in the 'beam off' condition. This is explained (as is the comparable observation with optical excitation) in terms of the conductivity induced in the copper compensated layer by the electron irradiation. This beam induced conductivity is the main reason why the characteristics of air-baked type A and type B cells measured under electron bombardment cross-over those measured in the dark (or under less energetic electron bombardment). With type A devices, apart from the introduction of the cross-over effect, the change in the shape of the characteristics and in the value of V_{oc} and I_{sc} was not significant. In fact undesirable changes in the absorption coefficient of Cu_xS with heat treatment are not important for electron beam irradiation. So that the value of I_{sc} generated by electron bombardment was not reduced after heat treatment as was the optically excited value.

With type B devices the 2 min air-bake led to a substantial increase in V_{oc} and the fill factor. Such an improvement is usually attributed to a decrease in the density of interface states[16]. This could perhaps explain the differences in the current-voltage characteristics for beams of different energy incident on the side of the hillock (light region) on type B devices before and after air-bake. For instance the presence of a higher density of interface states before heat treatment may explain why the V_{oc} generated by a 7.5 keV beam incident on the side of a hillock was smaller than the V_{oc} produced by 25 keV beam (Figs 6.6 and 6.11). After the heat treatment however, when the density of interface states was reduced the V_{oc} generated by both the 7.5 keV and 25 keV beams were of comparable magnitude indicating that interface states were now less important. This corresponds to the optical analogue where an increase in the intensity of illumination at least above a certain level increases I_{sc} but not V_{oc}[17].

(ii) Minority Carrier Diffusion Lengths

If the generation volume can be considered as a point source[18], the minority carrier diffusion length can be found directly from a plot of the logarithms of the beam induced current versus displacement from the junction. Shea et al [12] have shown that for higher beam energies a plot of log EBIC versus x is curved. Then the slopes do not have any direct relation to L_n or L_p. Furthermore, uncertainties due to recombination at the beam entry surface (perpendicular to the junction plane) and at the surface parallel to the junction plane influence the measured values of diffusion length considerably[19]. A detailed analysis of the resolution limits of the EBIC technique in the determination of diffusion lengths in semiconductors has been given by Shea et al[12]. They concluded that the electron range should remain less than 4 L if the true value of minority carrier diffusion length is to be measured. This criterion was developed from the EBIC profile of the lateral dose function (for details see Ref.(12)). For all our diffusion length measurements an electron beam energy of 7.5 keV was used. The R_G values for this beam energy are 0.392 μm in Cu_xS and 0.549 μm in CdS. Therefore true values of diffusion lengths as small as 0.01 μm and 0.137 μm may be measured in Cu_xS and in CdS (providing the beam diameter is smaller than these values).

Although several authors[15,19,20] have shown that the dependence of the collected current on the position of the point source generally deviates from the simple exponential function as a consequence of surface recombination, Berz and Kuiken[21] have demonstrated that the minority carrier diffusion length may still be measured even for a source located on the surface. Bresse and Lafeille[22] showed that the effect of surface recombination at the outer surface parallel to the junction, on the EBIC current, is considerably reduced for sources of minority carriers at a depth greater than the diffusion length. The thickness of the copper sulphide layers was found to be about $\sim$ 0.8 μm for a 20s dip in the standard solution, but

after cleavage the junction was not clearly defined, Fig 6.13 (a-b). With a plating time of 30s or longer, exposed junctions were well defined. However, by keeping the dipping time just long enough to obtain optimum conditions the migration of copper into the CdS during the plating was partially avoided. With no copper acceptors in the CdS, minority carriers created in CdS will not be subject to rapid recombination in the depletion region[23]. However, if a considerable concentration of acceptors is built up in the CdS by copper diffusion from Cu_xS, the electric field at the junction and throughout the depletion region decreases, or the high density of interface states reduces the effective barrier at the junction and leads to low junction field and a large tunnelling recombination current. Thus, in both cases, the recombination of carriers in the depletion region and the flow of electrons created in the CdS via interface states into the Cu_xS ought to be taken into account.

In Fig 6.17, a current trace is shown for a device fabricated on a mechanically polished surface of CdS by dipping for 30s in a standard solution. It is shown in Chapter 5 that mechanical polishing of single crystal CdS produces a polycrystalline sphalerite cubic surface layer. Moreover Oktik et al[24] have demonstrated that the displacement reaction between cuprous and cadmium ions is slower for copper sulphide layers formed on a polycrystalline CdS layer. Therefore the high value of L_p ($\sim$ 1.09 μm) in CdS for this device is attributable to the negligible amount of copper diffusion during plating. However, after an air-bake for 2 mins at 200°C, the value of L_p was reduced to 0.36 μm. This demonstrates the important effect copper levels in CdS have in the diffusion length. Obviously copper acceptor levels reduce the mobility of holes in CdS. The close relation between plating time and measured diffusion length in CdS can be seen from Table 1 (for as-made devices on etched and polished surfaces). Table 1 also shows clearly the effect air-baking has on L_p in CdS. After heat treatment the spread in measured values of L_p was reached.

In contrast the minority carrier (electron) diffusion length in Cu_xS did not change significantly, either as a function of preparation technique or after the post barrier air-bake (see Table 1). The average value of L_n in Cu_xS was about 0.23 μm. This value and the conclusion as to the effect of heat treatment on L_n in Cu_xS are in a good agreement with the work by Shea and Partain[25] and Partain et al[26] but in contrast with the reports by Windawi[27] and Rothwarf[28] who claimed that there was a change in the minority carrier lifetime in Cu_xS before and after heat treatment. However, it is assumed that the effect of this change on the L_n values in Cu_xS is far too small to measure within the accuracy of the EBIC techniques. Although the results of Partain[25,26] on L_n in Cu_xS agree with our observations, their results on L_p in CdS conflict with ours. They reported that the air-bake at 120°C and 200°C had no effect on the measured minority carrier diffusion length of 0.29 μm in CdS. Interestingly, their value for L_p matches quite well with the L_p value measured on heat treated samples in this work. This suggests that their preparation technique which is one hour dipping of polished surfaces in standard plating solution causes a large amount of Cu diffusion into the CdS.

In Fig 6.21 two different slopes occur in the plot of log EBIC versus beam distance on the CdS side. This could be the result of variations in surface recombination velocity at the beam entry surface. However, observation on newly exposed surfaces after heat treatment suggests that two slopes imply the existence of two adjacent regions of CdS with different properties. This can be caused by several factors, for instance, different defect configurations in these regions.

In summary our work reveals that the L_n value of $\sim$ 0.23 μm is relatively constant in Cu_xS regardless of device fabrication phase and post-treatments, whereas the values of hole diffusion length in CdS have a strong correlation with preparative procedures such as surface preparation

plating time, and the air-bake. In fact changes in the minority carrier diffusion length in CdS do not significantly affect the operation of the device as a solar cell, since most of the light is absorbed in the copper sulphide layer. Bragagnolo[29] has shown that only 2% of the light generated current comes from the CdS for an optimized cell. Thus the change in L_p in CdS can not account for the change in the cell parameters after heat treatment.

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CHAPTER 7

ANALYSIS OF CdS/Cu_2S JUNCTIONS

7.1 INTRODUCTION

In this chapter the mechanisms of dark current conduction are analysed in type A and type B devices in their as-prepared state, and after a post barrier air-bake, in an attempt to improve our understanding of the electrical characteristics of these cells. In section 7.2 a study of the current-voltage characteristics of both types of device at several temperatures is presented. In addition the barrier heights determined by various techniques are also discussed. Section 7.3 describes the effects of a post barrier air-bake on the current transport in both types of device, and in the following section measurements on the junction capacitance are presented which provide information pertinent to the space charge region and the junction parameters. The analysis of photocapacitance spectra and infrared quenching effects in heat treated cells forms the subject matter of section 7.5. In section 7.6 the experimental observations are discussed in terms of a model which is proposed for the as-made and heat treated cells.

7.2 INVESTIGATION OF THE DARK CONDUCTION PROCESS IN AS-MADE CdS/Cu_2S HETEROJUNCTIONS

Current-voltage characteristics of CdS/Cu_2S heterojunctions have been studied in an attempt to establish the dark conduction mechanisms in these devices. Measurements were carried out over the temperature range from 85 K to 300 K.

In Fig 7.1 the forward and reverse current-voltage characteristics of an as-prepared type A device, measured in the dark at room temperature, are plotted semi-logarithmically. The forward current which is typical of most devices consists of three regimes. In the region I ($V_F \lesssim 0.15$ V) the forward conduction mechanism obeys a simple ohmic law. In fact in this

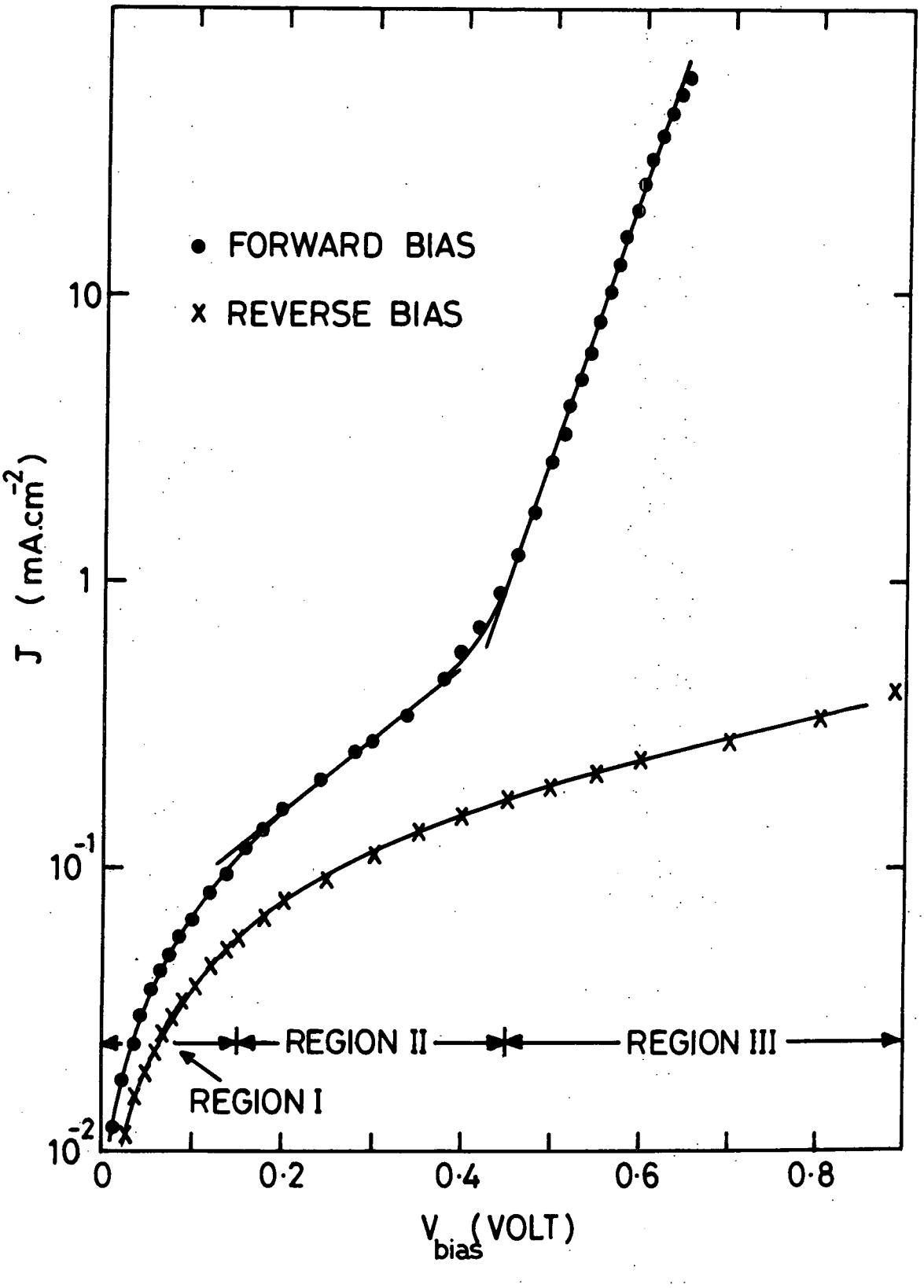

FIG. 7·1 DARK CURRENT - VOLTAGE CHARACTERISTICS FOR AN AS-MADE TYPE A CELL AT ROOM TEMPERATURE

region the reverse current characteristic is very similar to that measured in forward bias. With increasing forward bias, the forward current, J_F, exhibits two distinct branches with two different slopes. In general at forward bias voltages larger than 3 kT/q many heterojunctions obey an empirical relation of the form,

$$J_F = \underbrace{J_{OO} \exp\left(\frac{-\Delta E}{kT}\right)}_{J_o} \exp\left(\frac{qV}{AkT}\right) \qquad (7.1)$$

where J_{OO} is defined by the type of conduction process, and ΔE is the energy at which the space charge region is thin enough to permit tunnelling of electrons to the empty interface states for this process. The rest of the symbols have their usual meanings. If regions II and III are fitted to Eq. 7.1, the values of the diode factor, A, calculated from the slope of these straight lines, and of the current factor, J_o, obtained by extrapolating the straight lines to zero bias are given in Table 7.1 for this particular device.

REGION	slope = $\left(\frac{q}{AkT}\right)$ (V^{-1})	Diode factor (A)	Current factor (J_o) (mA cm^{-2})
II	5.76	6.81	$5.95\ 10^{-2}$
III	22.10	1.77	$3.02\ 10^{-5}$

TABLE 7.1 : Typical parameters for a type A cell in the as-made condition, measured at room temperature.

The reverse bias current did not reach saturation. The log-log plot of J_R-V_R in Fig 7.2 demonstrates that the reverse characteristics of type A devices can, in general, be described by an expression of the form

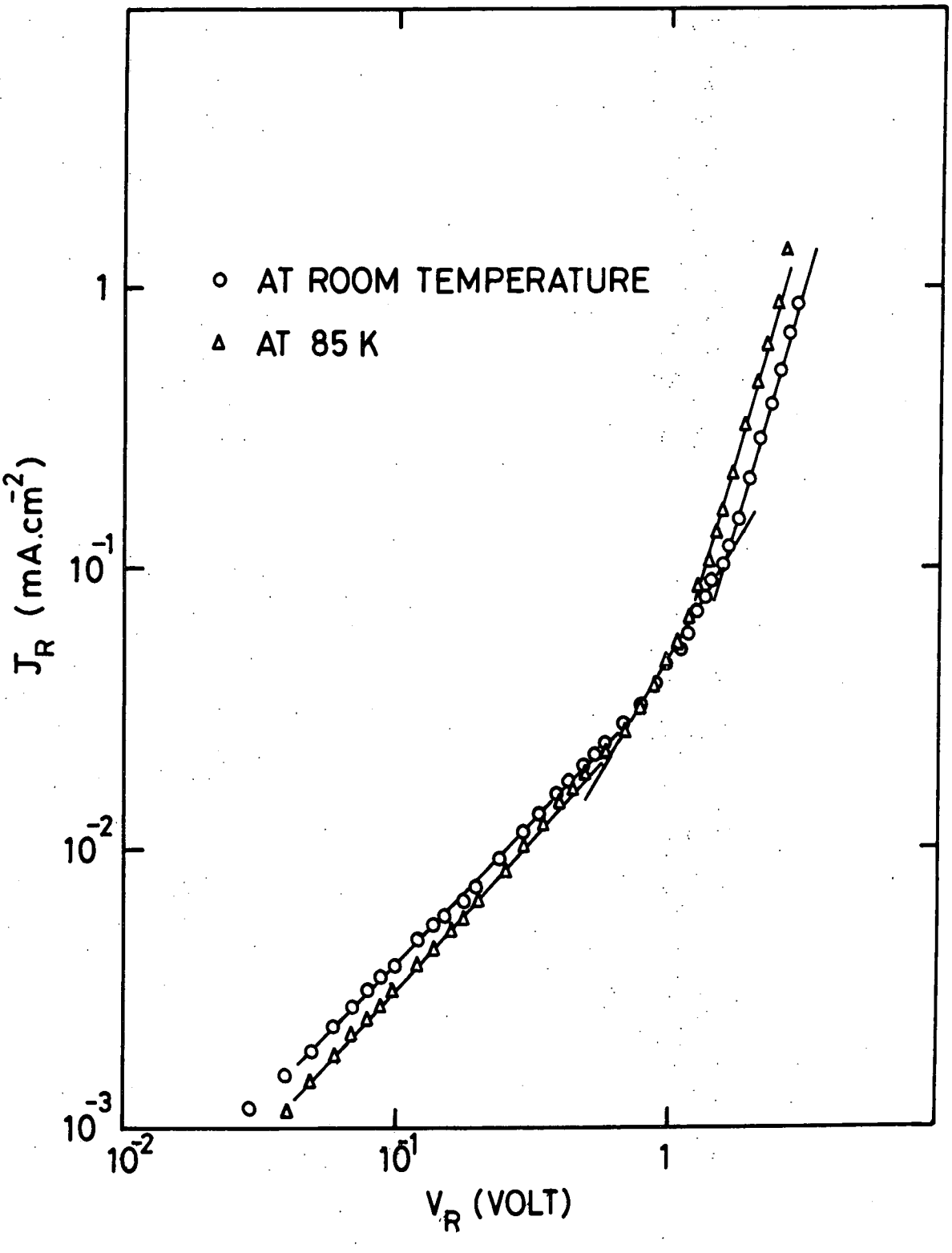

FIG. 7·2 LOG-LOG PLOT OF DARK REVERSE CURRENT-VOLTAGE CHARACTERISTICS FOR AN AS-MADE TYPE A CELL

$J_R \propto V_R^{\gamma}$. At low voltages with V_R up to 0.5 V γ calculated from the slope was 1.0 and in the second region for V_R between 0.5 and 1.7 V, γ was 2.0. With voltages in excess of 1.7 V a third region appeared with a γ value of 3.0. Thus the reverse current for biases exceeding 0.5 V was compatible with zener effect ($J_R = B V^{\gamma}$, $\gamma \geq 2$).

In order to explore the dark current mechanisms further, forward bias data shown in Fig 7.3 were taken between 85 K and 295 K. Typical three region characteristics were observed at all temperatures. However, the variation of J_F with temperature was of different form in the three regions. The temperature dependence of J_F at three different fixed forward bias voltages (+ 0.2 V, + 0.4 V and + 0.6 V) is shown in Fig 7.4. In region I, ($V_F \lesssim$ 0.15 V) the excess current flowing through the junction was only slightly temperature dependent. At + 0.2 V bias, J_F showed two distinct regions, and at + 0.4 and + 0.6V three regions were observable in the range 85 K to 330 K. Moreover the onset of the various regions started at lower temperatures as the forward bias was increased. However the slopes of the log J_F versus V_F plots in both regions II and III were practically constant (see Fig 7.3). A small change in these slopes can be explained in terms of the temperature dependence of the bandgaps of the materials, for instance dEg/dT is about $-5.2\ 10^{-4}$ eV/kT for CdS[1]. The diode factor, A, and current factor, J_o, measured at temperatures in regions II and III are tabulated in Table 7.2 for this particular device in as-made condition.

	Temperature (K)	Slope (α) (V^{-1})	A = ($q/\alpha kT$)	J_o (mA cm^{-2})
REGION II	295	5.15	7.64	$5.95\ 10^{-2}$
	227	5.00	10.22	$5.35\ 10^{-2}$
	196	5.10	11.60	$4.95\ 10^{-2}$
	137	5.20	16.30	$4.39\ 10^{-2}$
	85	5.30	25.76	$3.34\ 10^{-2}$
REGION III	296	22.10	1.77	$3.02\ 10^{-5}$
	227	24.80	2.06	$1.14\ 10^{-6}$
	196	25.20	2.34	$1.31\ 10^{-7}$
	137	26.00	3.25	$8.30\ 10^{-8}$
	85	26.60	5.13	$5.08\ 10^{-8}$

TABLE 7.2: The variation of current and diode parameters with the temperature for as-formed type A cell.

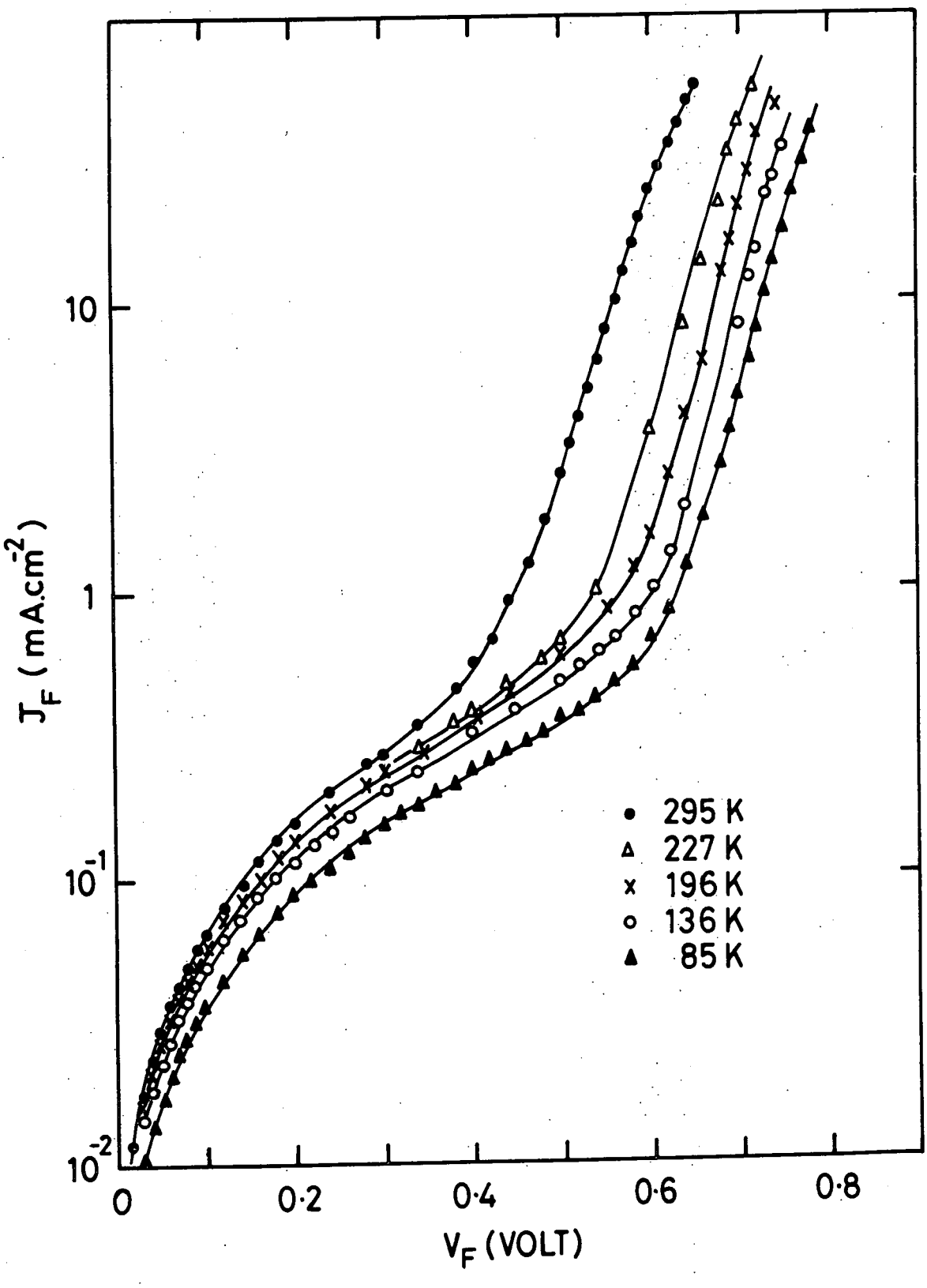

FIG. 7·3 DARK CURRENT - VOLTAGE CHARACTERISTICS FOR AN AS-MADE TYPE A CELL AT DIFFERENT TEMPERATURES

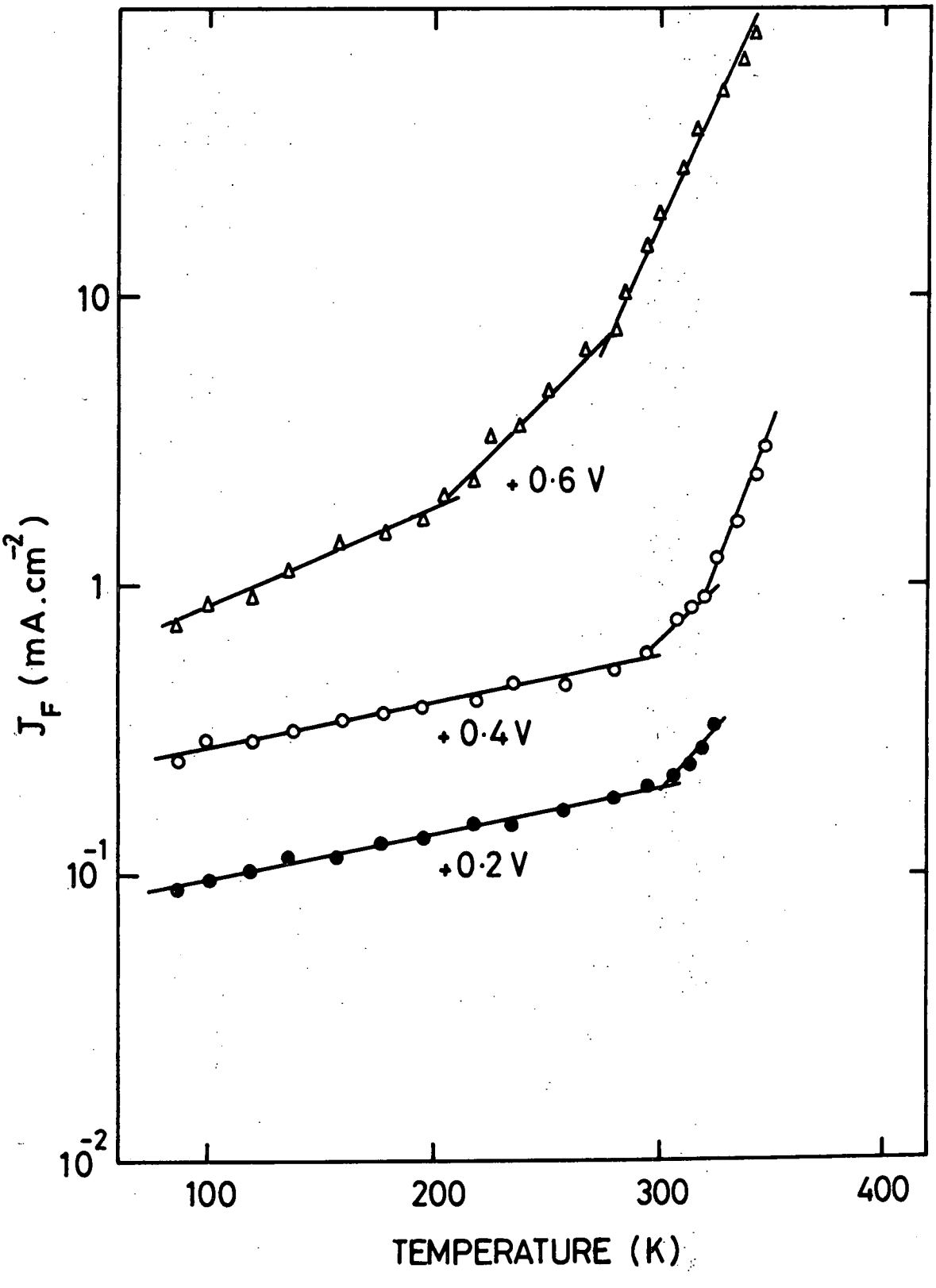

FIG. 7·4 DARK FORWARD CURRENT - TEMPERATURE CURVES FOR AN AS-MADE TYPE A CELL AT DIFFERENT FIXED FORWARD BIAS VOLTAGES

In general, all type A devices exhibited similar characteristics in region III, but their parameters in region II ($0.2<V_F<0.4$ V) varied from device to device with values of A, ranging from 3 to 8, and of J_o varying from 10^{-3} mA cm^{-2} to 1 mA cm^{-2} at room temperature. Nevertheless the slopes of the characteristics were always temperature independent.

The variation of the current factor, J_o, with temperatures is plotted semilogarithmically for region II and III in Fig 7.5. In region II J_o showed a very weak temperature dependence from 85 to 300 K but in region III the variation of J_o, although weak in the range 85 K to 200 K, was quite rapid at higher temperatures. Because of lack of information about the temperature dependence of the pre-exponential factor J_{oo}, a value of the activation energy could not be calculated from this plot. However, the temperature independent slopes of the log J_F vs V plots in regions II and III suggest that two independent conduction mechanisms involving thermal activated tunnelling recombination are operative, so that the forward bias current-voltage relation can be written

$$J_F = \underbrace{q\, N_C\, S_I}_{J_{oo}} \exp\left\{ - \frac{(\Delta E - qV/A)}{kT} \right\} \qquad (7.2)$$

where S_I is the interface recombination velocity and N_C is the effective density of states for CdS $\left(= 2\,(2\pi m^* kT\, h^{-2})^{3/2} \right) \sim 2.3\ 10^{18}$ cm^{-3} at room temperature. The other symbols have their usual meanings. In the pre-exponential coefficient J_{oo}, N_C varies as $T^{3/2}$, and assuming that as S_I depends on temperature as $S_I \propto T^{\frac{1}{2}}$, J_{oo} can be rewritten as $J_{oo} = J_{oo}' T^2$, where J_{oo}' is a constant.

Hence the activation energies of the current transport processes can be inferred from plots of log J_F/T^2 vs T^{-1}. Fig 7.6 shows such plots at three forward biases (+ 0.2, + 0.4, + 0.6 V) in the range 85-330 K.

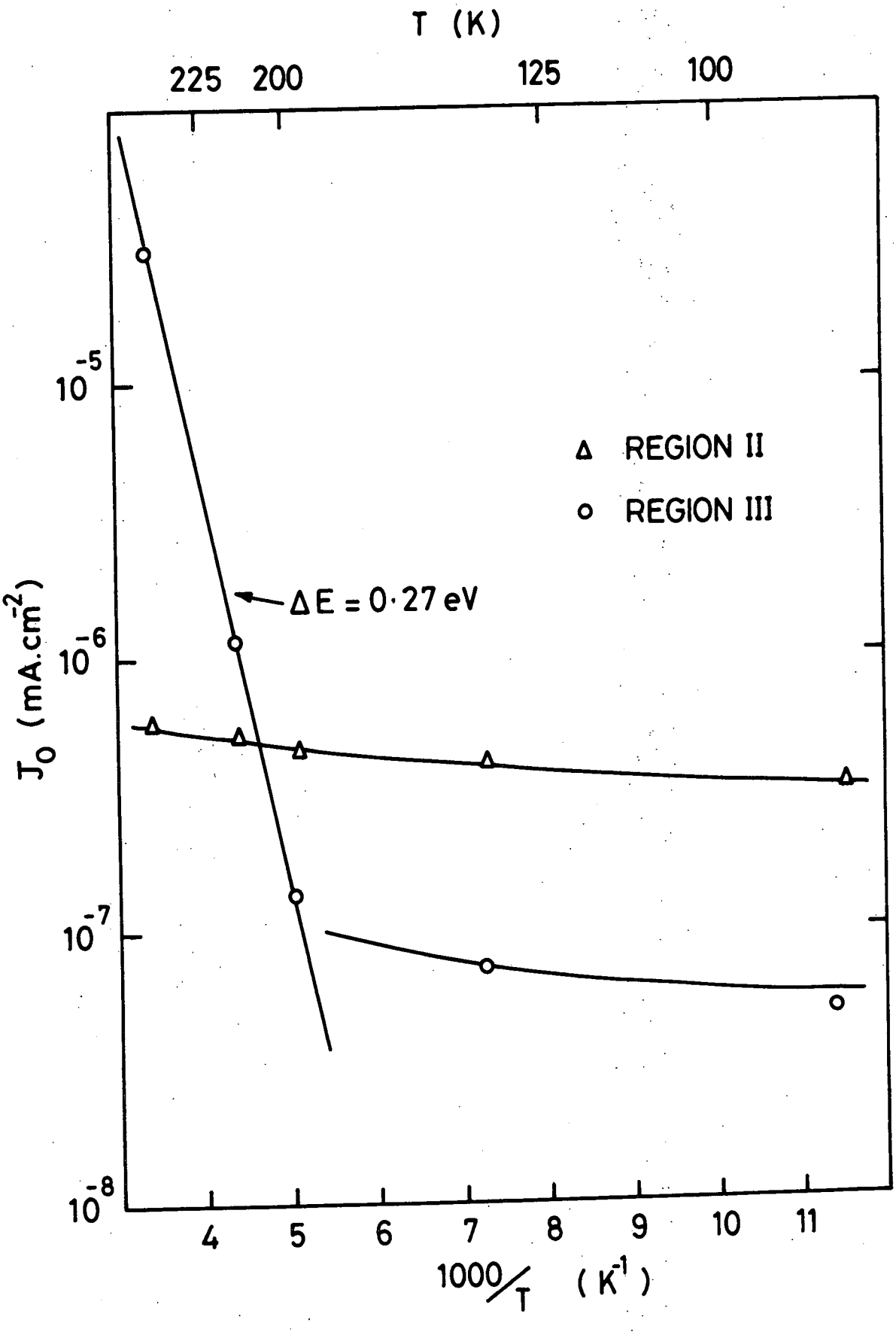

FIG. 7·5 PLOT OF CURRENT FACTOR, J_0, AS A FUNCTION OF $1/T$ FOR AN AS-MADE TYPE A CELL

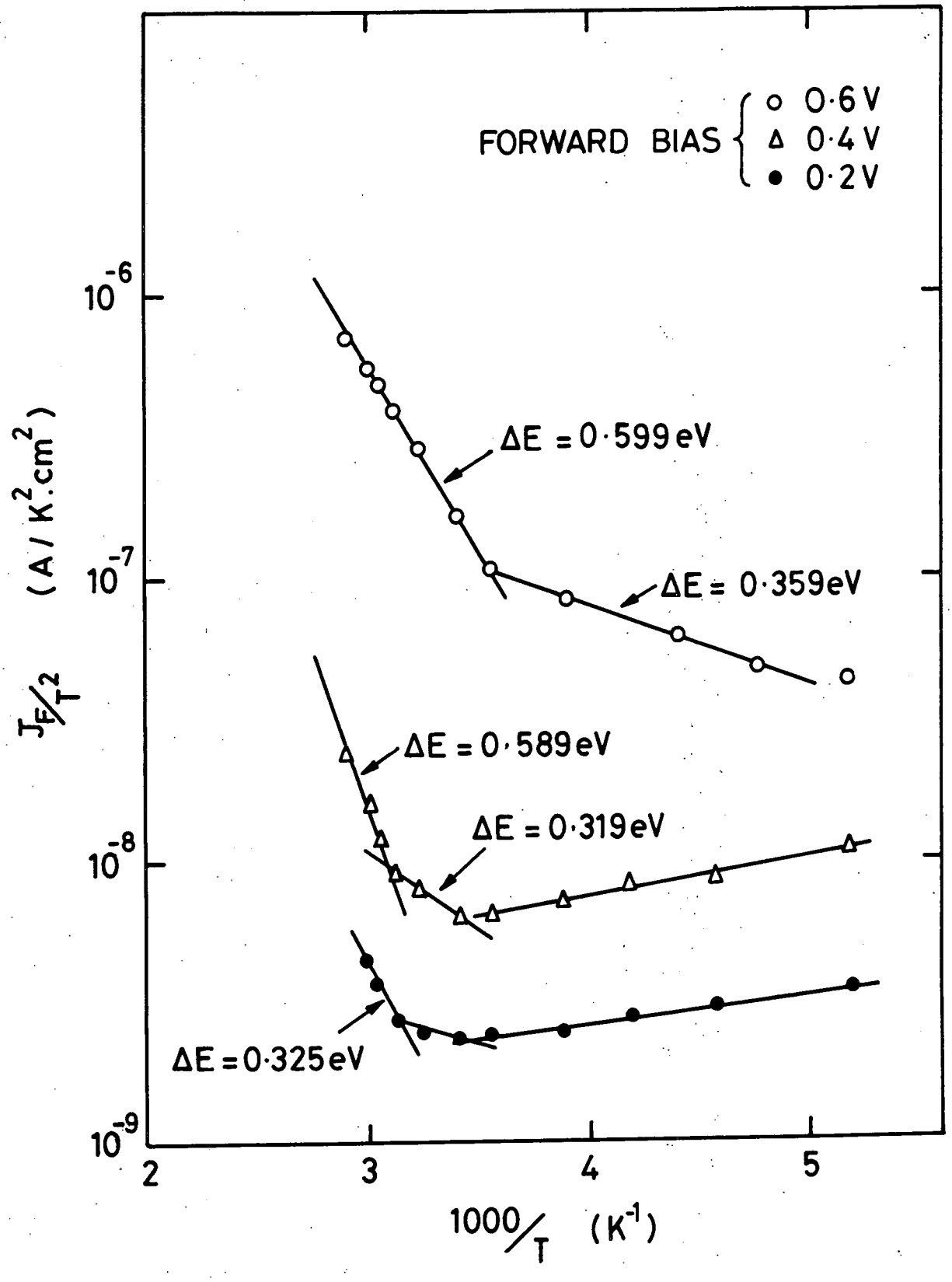

FIG. 7·6 ARRHENIUS - TYPE ACTIVATION PLOTS OF STEADY FORWARD DARK CURRENTS FOR AN AS-MADE TYPE A CELL AT THREE FIXED BIASES

A difficulty arises with this type of analysis in CdS/Cu_2S junctions due to the rapid diffusion of copper from the copper sulphide into the CdS, with consequent changes in the junction profile as the temperature is increased above room temperature. Thus it is practically impossible to make activation energy studies on a cell with the same properties at higher temperatures. In order to avoid such complexities the upper temperature limit was restricted to room temperature. Up to this temperature plots of log J_F/T^2 versus T^{-1} exhibited two distinctive slopes at forward biases of + 0.4 and + 0.6 V. At + 0.2 V there was only one slope. The activation energies calculated from these curves for as-prepared type A devices, indicate that electrons, activated thermally to the energies at about 0.32 and 0.60 eV above the conduction band are directly accepted into the recombination centres located at or in the vicinity of the junction interface. Although the presence of interface states complicates the determination of the barrier height from current-voltage measurements in these devices, approximate values can be obtained by using a reasonable estimate of the interface recombination velocity. If S_I is assumed to be about 5 x 10^6 cm/s[2], the effective barrier height inferred from the J_o values of the sample whose characteristics are depicted in Fig 7.1 were ϕ_{II} = 0.6 eV from region II and ϕ_{III} = 0.8 eV from region III. There is a close similarity between the value of ϕ_{II} and the activation energy usually found in the vicinity of room temperature.

The reverse current for biases up to -1.0 V was almost temperature independent, but at higher voltages the reverse currents measured at low temperatures were larger than those measured at higher temperatures. These characteristics are also shown in Fig 7.2 (triangles). It is clear from this plot that the mechanisms at low temperatures are similar to those at room temperature. In as-prepared type A devices characteristics measured under AM1 illumination yielded a fill factor of about 0.70. Such a value suggests very low series and shunt losses (see Chapter 3, Fig 3.3(b)). Thus the

current under illumination can be written as the superimposition of the diode and short circuit currents as in Eq. 3.29, Chapter 3. When J_{sc} is large compared with J_o the open circuit voltage is a modified version of Eq. 3.30

$$V_{oc} \simeq \frac{AkT}{q} \ln\left(\frac{J_{sc}}{J_o}\right) \tag{7.3}$$

so that the measurement of J_{sc} and V_{oc} as a function of light intensity will yield a current factor, J_o, and a diode factor, A, if Eq.7.3 holds.

Fig 7.7 is a plot of log J_{sc} versus V_{oc} for an as-made type A cell as the intensity of illumination was increased from 1 to 100 m W cm^{-2}. The light intensity was varied by placing neutral filters in front of the cell. The straight line indicates that the relation in equation 7.3 holds perfectly in this range, and values of A = 1.65 and J_o = 2.03 10^{-4} mA cm^{-2} result. By using this J_o value in Eq. 7.2 the barrier height under illumination turns out to be 0.76 eV for this particular device.

Photothreshold measurements at zero bias have also been made on type A cells to determine the barrier height for the combined effects of photo-excitation of electrons from the valence band of the Cu_xS to the interface states and tunnelling to the CdS conduction band. If the photoresponse R(hν) is defined as the photocurrent per absorbed photon of energy hν, then a plot of $\sqrt{R}$ versus hν may be used to define an apparent barrier height[3]. A calibrated PIN diode was used to ensure that a constant energy of incident light at each wavelength could be obtained. Fig 7.8 shows the square root of the photoresponse at zero bias as a function of quantum energy in the near infrared region for as- made type A device. The straight line gives an extrapolated value of 0.85 eV on the energy axis. Threshold values measured in this way varied from 0.85 to 0.92 eV for the type A cells examined.

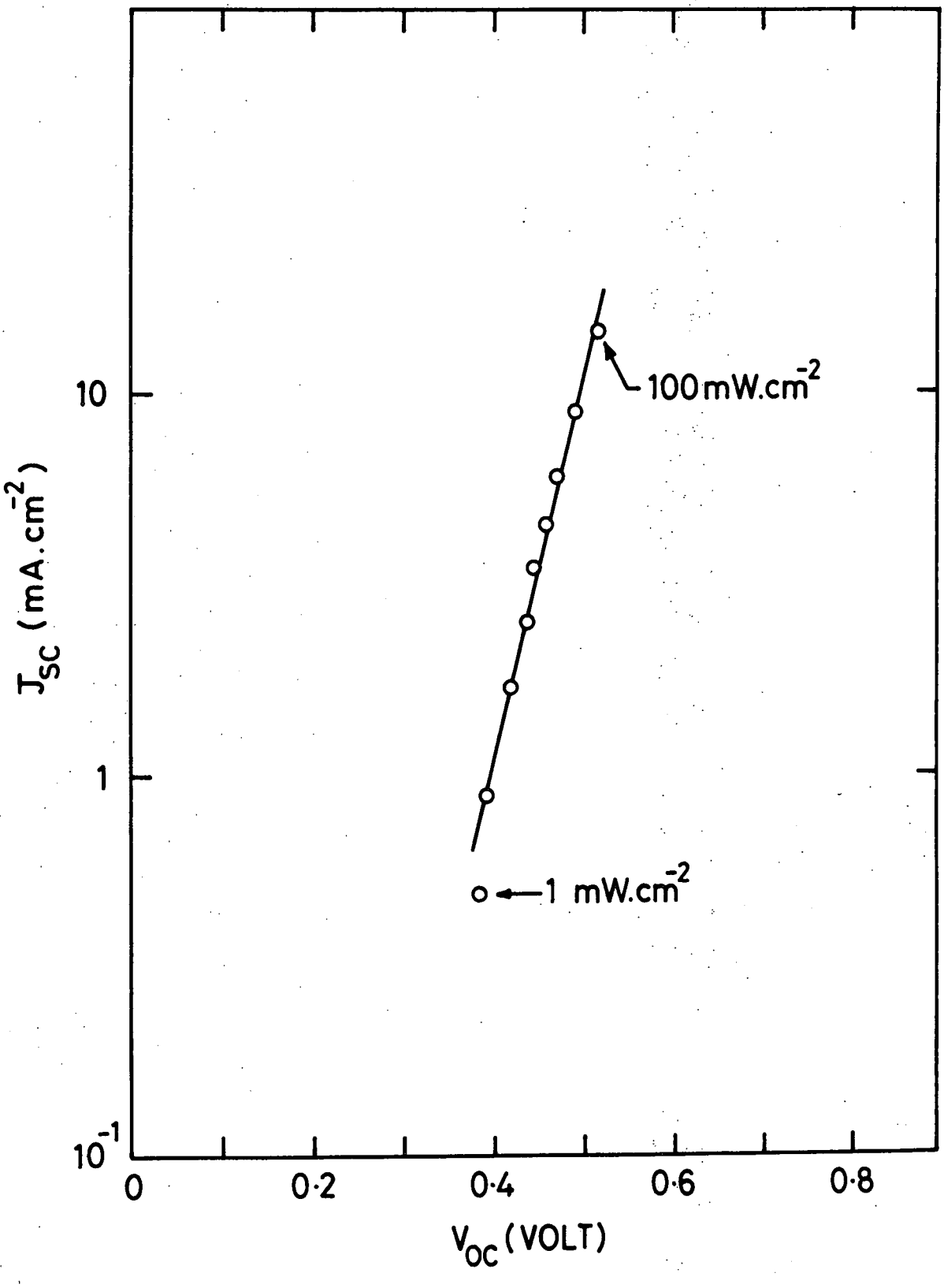

FIG. 7·7 THE DEPENDENCE OF SHORT-CIRCUIT CURRENT ON OPEN CIRCUIT VOLTAGE AS A FUNCTION OF INTENSITY FOR AN AS-MADE TYPE A CELL

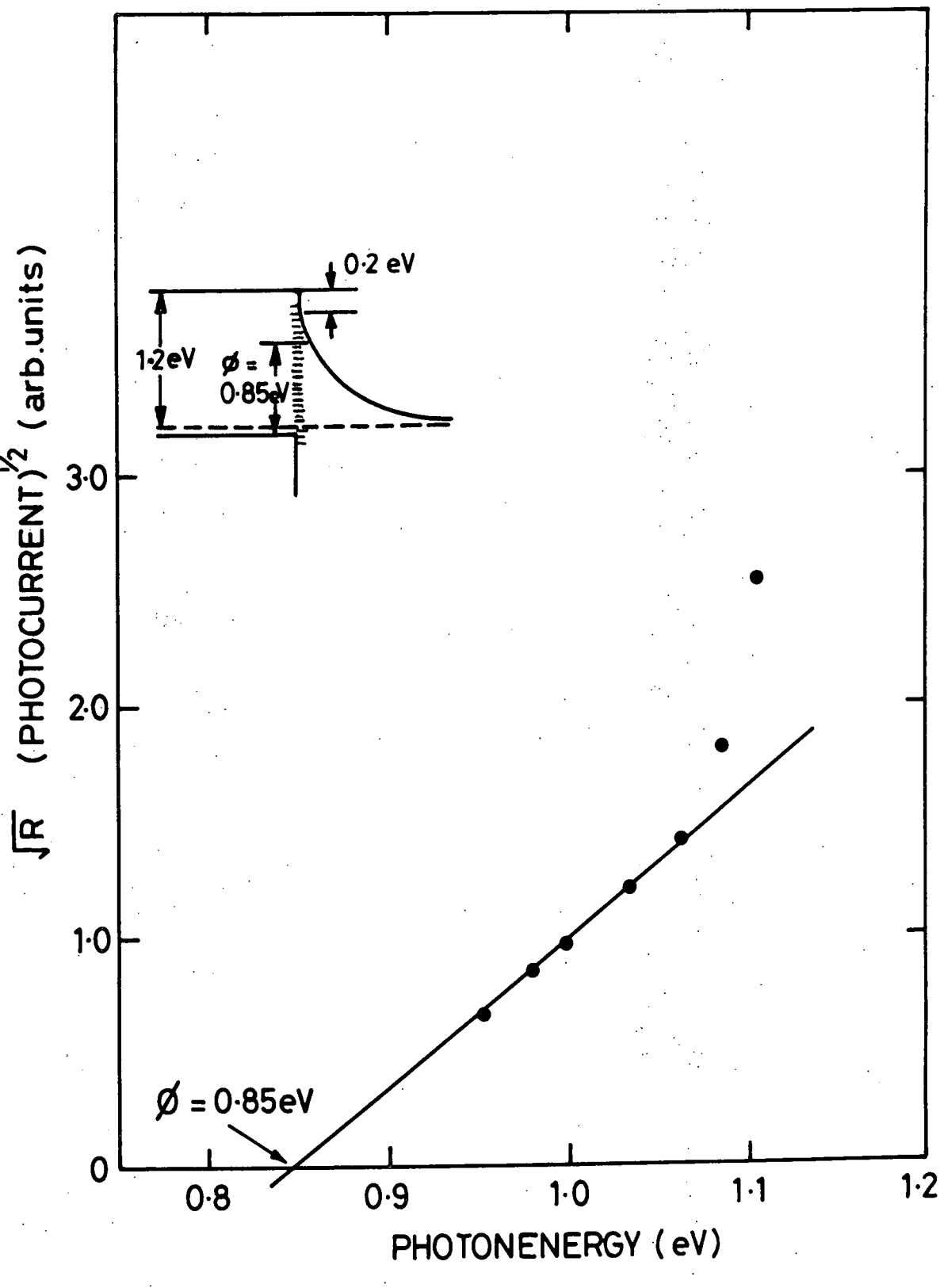

FIG. 7·8 SQUARE ROOT OF THE CORRECTED PHOTOCURRENT VERSUS PHOTON ENERGY FOR AN AS-MADE TYPE A DEVICE

Values of barrier height for four type A as-made CdS/Cu_2S devices obtained using the various methods of analysis are summarized in Table 7.3

Method Applied	Measured Barrier Heights at 296 K ϕ_B (eV)			
	HET706/3	HET713/2	HET727/8	HET706/10
J_F-V_F (Region III)	0.80	0.81	0.83	0.82
J_{sc}-V_{oc} (Different Intensity)	0.76	0.79	0.77	0.78
$J_{sc}^{\frac{1}{2}}$- hν	0.85	0.92	0.87	0.88

TABLE 7.3: Measured barrier heights for as-made type A CdS/Cu_2S cells.

As stated earlier, type B devices have very poor diode and photovoltaic behaviour in their as-prepared state. The very low fill factor (AM1) of these cells indicates that a considerable proportion of the loss occurs by junction leakage (or shunting paths). Typical dark current-voltage characteristics at 85 and 296 K for a type B device are plotted semi-logarithmically in Fig 7.9. It is again clear that type B cells exhibit two different regions in the dark forward J-V characteristics. Region II dominates the current transport mechanisms between + 0.20 and + 0.75 V. The slope and diode factor, A, in this region at 296 K are 3.62 and 10.8 respectively. The current factor, J_o, calculated by extrapolating the straight line to zero voltage was 4.5 mA cm^{-2}. However, the slopes of the log J_F vs V_F plots at 85 and 296 K were practically the same. This and the weak temperature dependence of J_F are characteristics of tunnelling limited currents. Thus if Eq.7.2 is applied to this data a barrier height of

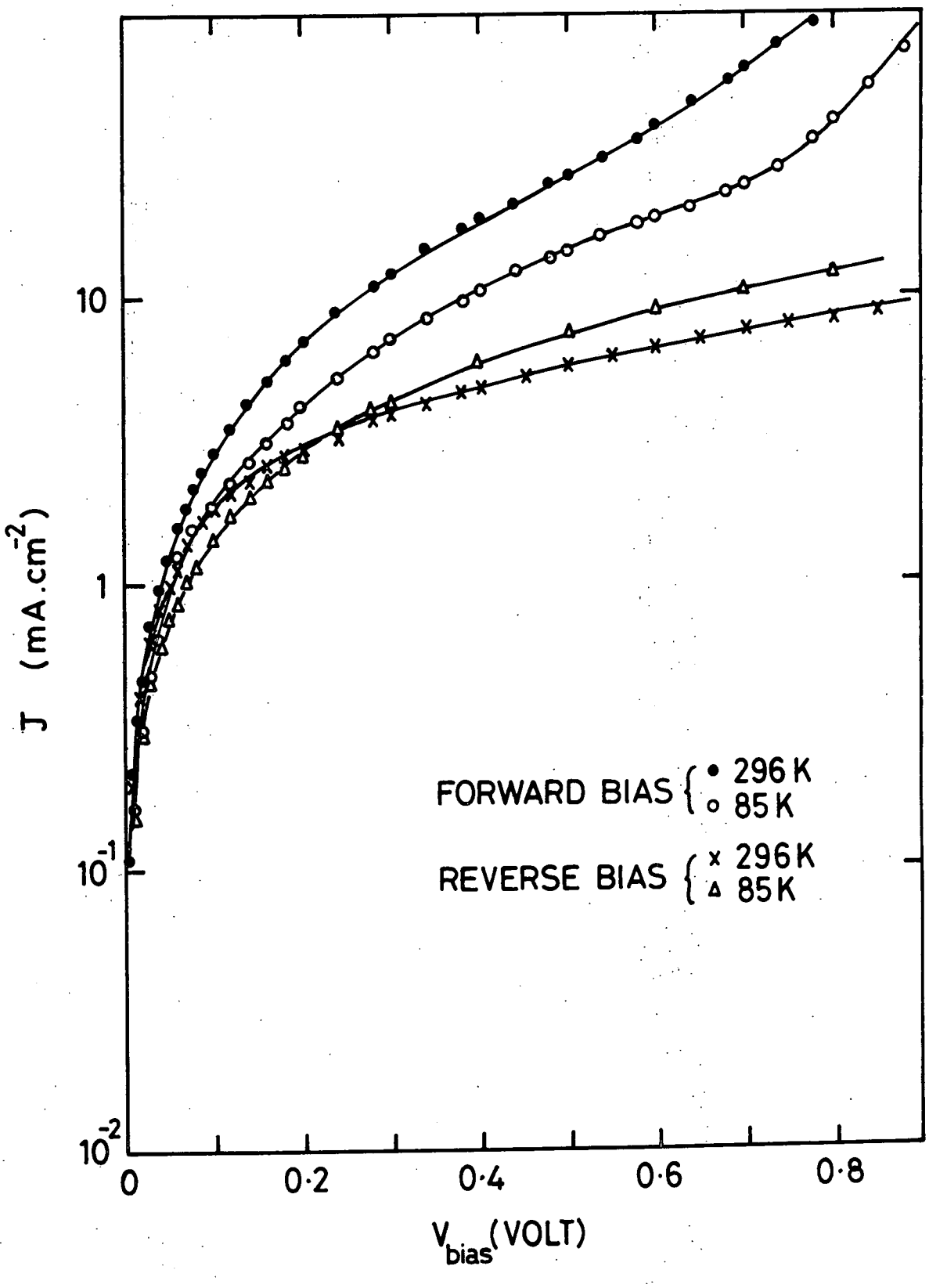

FIG. 7·9 DARK CURRENT - VOLTAGE CHARACTERISTICS FOR AN AS-MADE TYPE B CELL AT 85K AND 296K

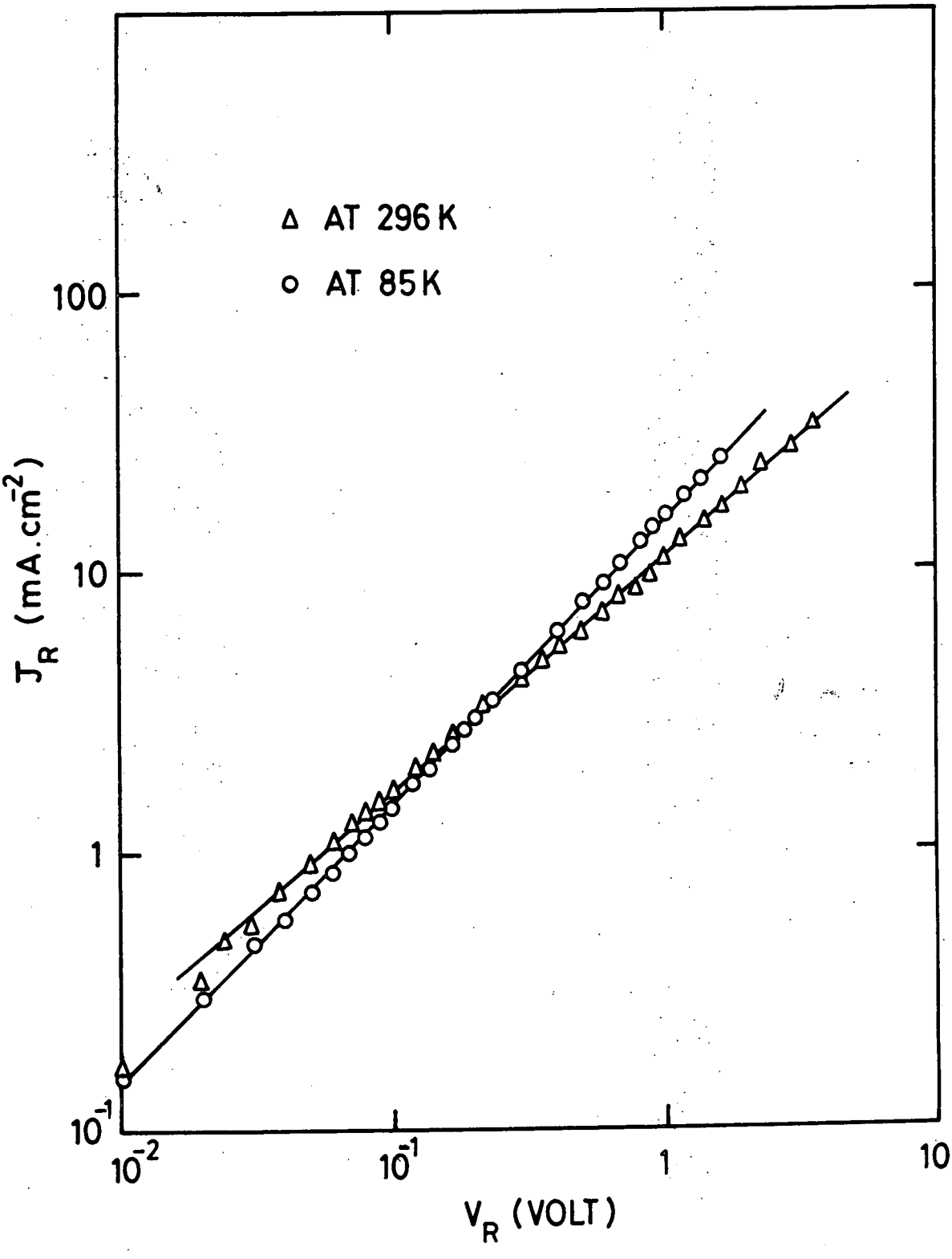

FIG. 7·10 LOG - LOG PLOT OF DARK REVERSE CURRENT - VOLTAGE CHARACTERISTICS FOR AN AS-MADE, TYPE B CELL AT 85K AND 296K.

0.51 eV is calculated for this particular type B device in its as-made condition.

Typical dark reverse currents, J_R for type B cells are also shown in Fig 7.9. The first observation is that the magnitudes of the reverse currents of these cells were two orders of magnitude higher than those for type A cells. Fig 7.10 demonstrates that the reverse current-voltage curves for type B devices can be described by the relation $J_R \propto B V_R^{\gamma}$ over three orders of magnitude of current. The temperature dependence of the reverse current was small, but the cross-over effect was also observed with the J_R-V_R characteristics measured at different temperatures for type B devices. As explained in Chapter 5, poor rectifying behaviour of type B devices improves with a decreasing number of ledges and kink sites on this type of surface. For instance Fig 7.11 shows the results obtained from an as-made type B cell with a relatively low density of ledges and kink sites on etch hillocks. Comparison of J-V characteristics in Figs 7.9 and 7.11 gives further confirmation of the direct correlation between surface features and the diode behaviour. Plots of the forward currents at fixed biases (+ 0.2 and + 0.4 V) as a function of temperature are shown in Fig 7.12. The lack of temperature dependence clearly indicates that the current mechanisms in this type of heterojunction are dominated by tunnelling. Because of the poor diode and photovoltaic behaviour of type B devices, the investigation of their parameters has not been pursued further.

7.3 EFFECTS OF POST BARRIER AIR-BAKE ON DARK CONDUCTION PROCESSES

The heating of the samples above room temperature was carefully avoided, while the as-prepared devices were being examined in the dark and under 100 mW cm^{-2} illumination. When all necessary measurements had been completed on as-made cells, both types of devices were given an air-bake at 200^{o}C for 2 minutes.

Typical examples of the current voltage characteristics for type A cells measured at 85 and 296 K after air-baking are shown in Fig 7.13.

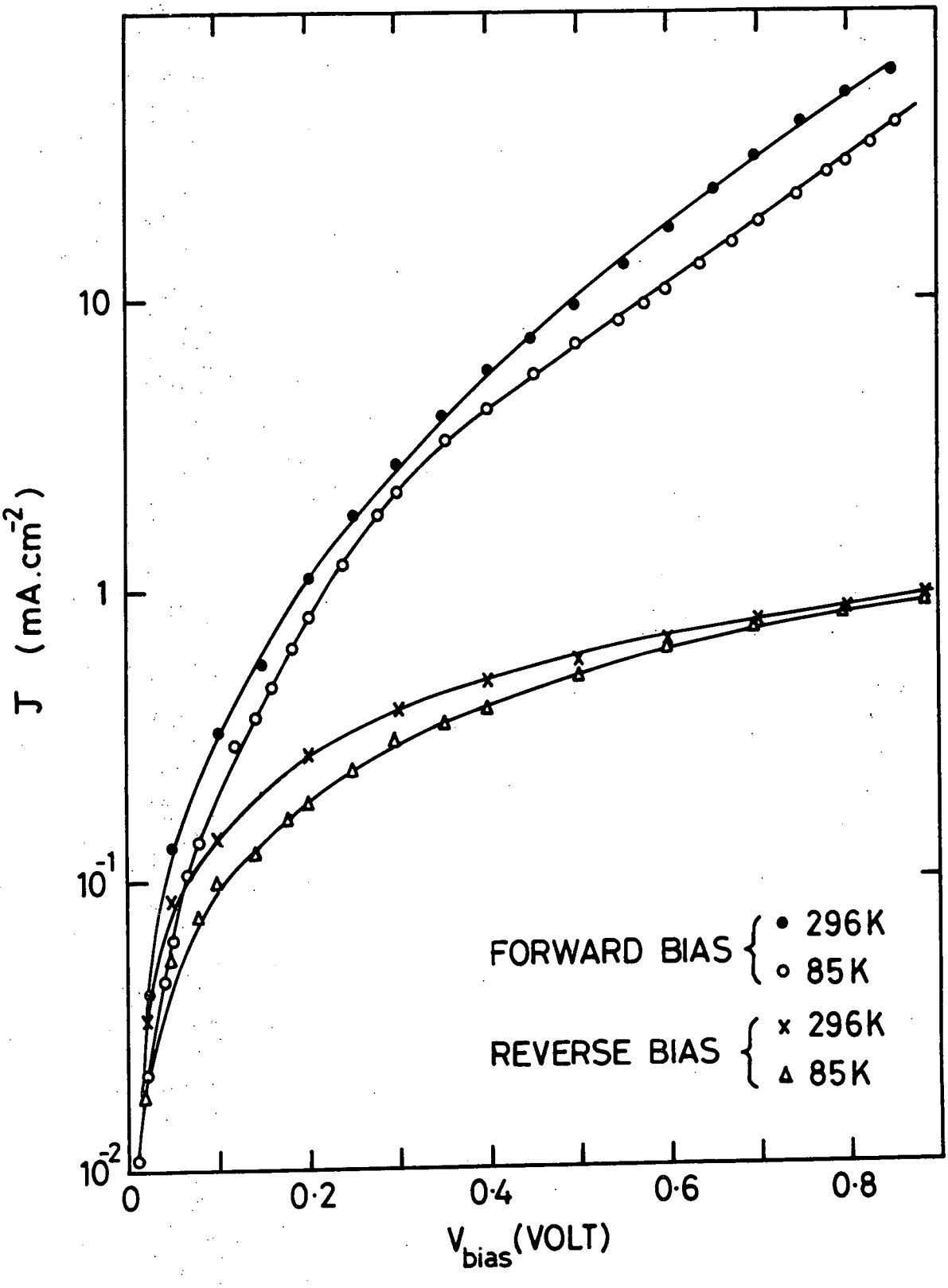

FIG. 7·11 DARK CURRENT - VOLTAGE CHARACTERISTICS FOR AN AS-MADE TYPE B DEVICE CARRYING A LOWER DENSITY OF LEDGES AND KINK SITES THAN THE DEVICE GIVING RISE TO THE CHARACTERISTICS IN FIG. 7·9

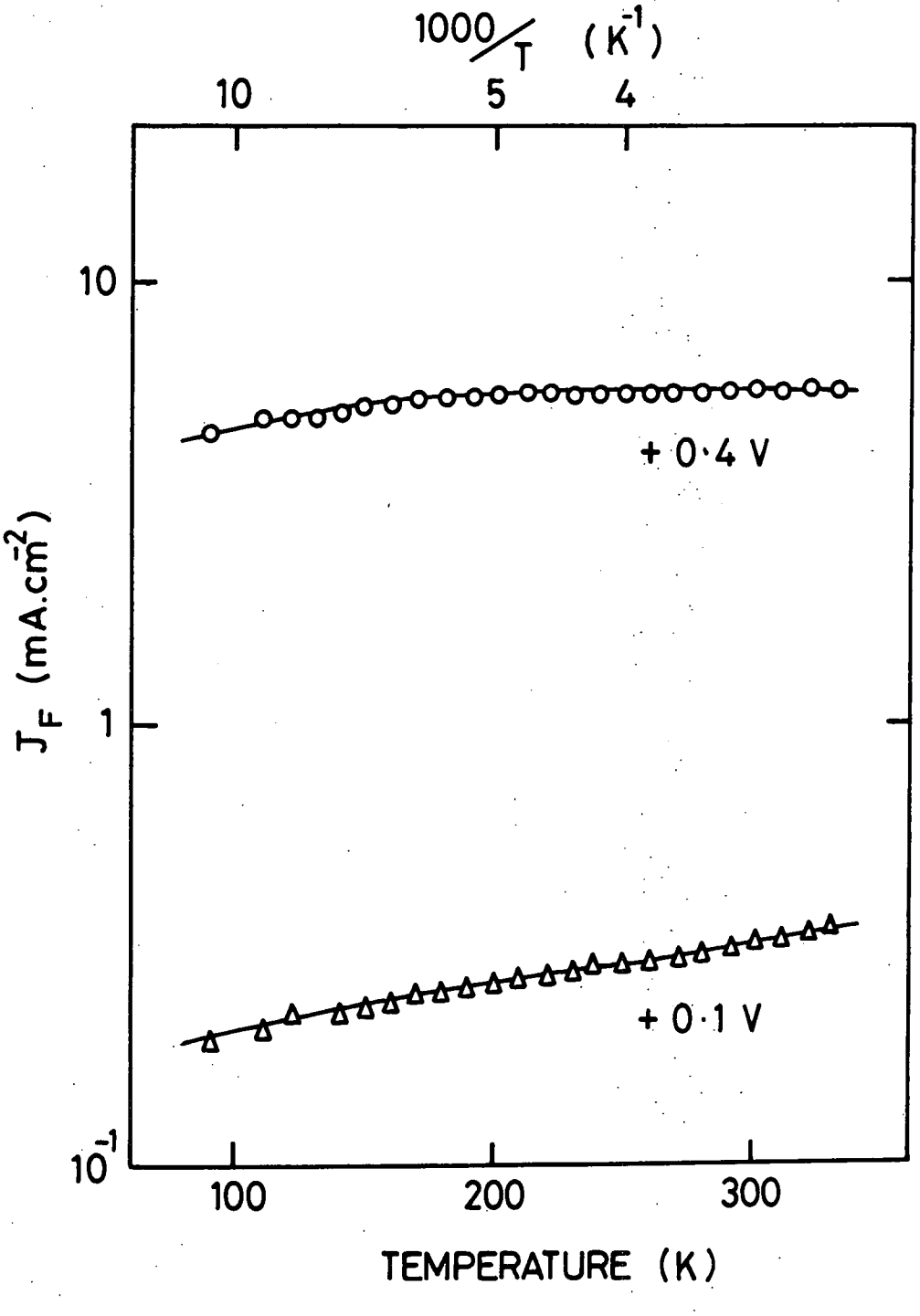

FIG. 7·12 DARK FORWARD CURRENT - TEMPERATURE CURVES FOR AN AS-MADE TYPE B CELL AT TWO FIXED FORWARD BIAS VOLTAGES

It was generally found that the current-voltage characteristics of type A cells measured at room temperature showed three regimes after the air-bake. Again with forward biases lower than 0.15 V (region I) the current followed a simple ohmic law but its magnitude was reduced by two orders. In region II the current was also two orders of magnitude less than that in as-prepared condition. In region II the diode factor improved from 7.7 to 6.9, the current factor from 5.95 10^{-2} to 1.89 10^{-4} mA cm^2, and the barrier height from 0.61 to 0.76 eV after a 2 minutes air-bake. As with as-prepared devices, the parameters derived in region II showed quite a spread after the heat treatment.

The onset of region III was also shifted down by two orders of current magnitude, and the characteristics in this region showed a diode factor close to unity ($A \tilde{\sim} 1.2$) and a J_o value of 2.46 10^{-8} mA cm^{-2}. The air-bake also increased the effective barrier height for this region from 0.80 to 0.99 eV. The current-voltage characteristics measured at different temperatures almost followed each other with a small divergence at low (10^{-4} mA cm^{-2}) and high (10^{2} mA cm^{-2}) values of the forward current. The variation of reverse current with applied voltage for heat-treated type A cells again exhibited three different regimes similar to the characteristics of the as-made devices (see Fig 7.14),although the total reverse current density was two orders of magnitude smaller. The temperature dependence of the reverse current was less at higher reverse biases and the cross-over effect occurred at about $\sim$ 2.5 V.

Typical forward current-voltage characteristics for a heat treated type B cell at two temperatures (85 and 296 K) are plotted semilogarithmically in Fig 7.15. Plots of log J_R versus log V_R for a heat treated type B cell, measured at 85 and 296 K, are shown in Fig 7.16.

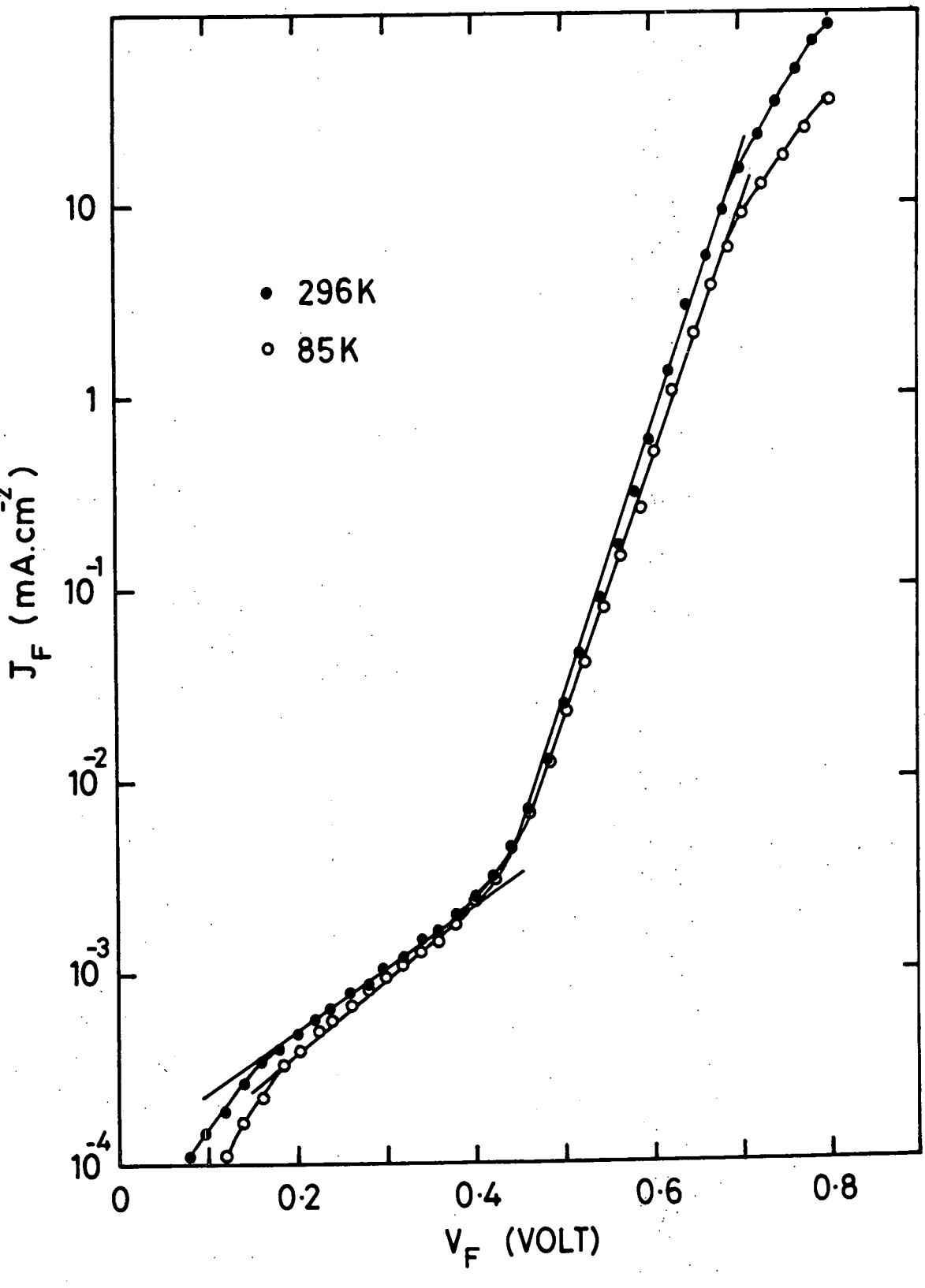

FIG. 7·13 DARK FORWARD J_F / V_F CHARACTERISTICS FOR A TYPE A CELL AFTER A TWO MINUTE AIR-BAKE

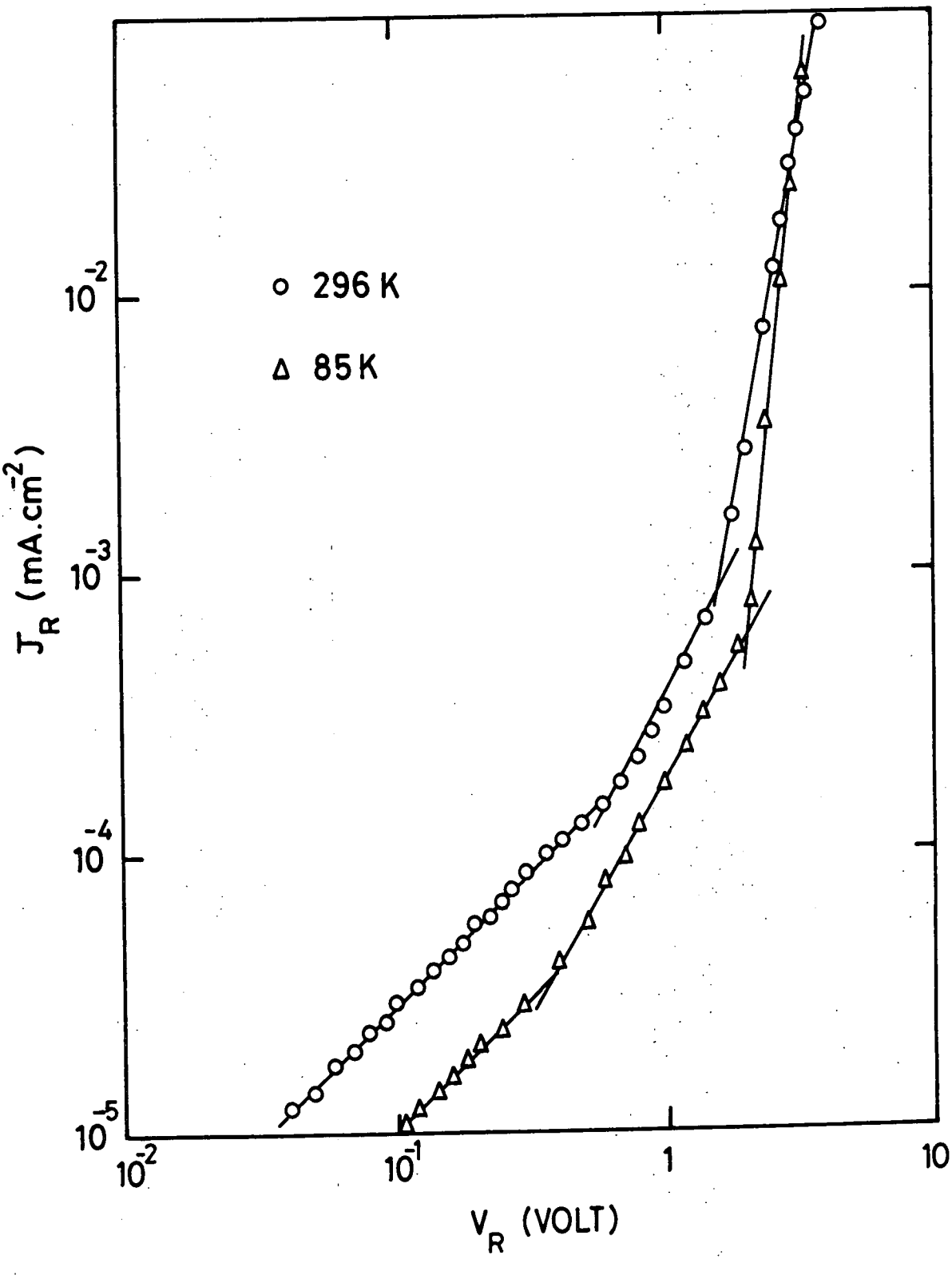

FIG. 7·14 LOG - LOG PLOT OF THE DARK REVERSE J_R / V_R CHARACTERISTICS FOR A TYPE A CELL AFTER A TWO MINUTE AIR-BAKE

It is clear from comparing Figs 7.13 and 7.15 and Figs 7.14 and 7.16, that there are close similarities between the forward and reverse characteristics of both types of device after the heat treatment. Calculated values of the diode parameters of baked devices gave further confirmation of the comparability of both types of junction in the dark. The values found for regions II and III of both types of device are listed in Table 7.4.

Parameters	TYPE A		TYPE B	
	Region II	Region III	Region II	Region III
J_o (mA cm^{-2})	1.89 10^{-4}	2.46 10^{-8}	6.86 10^{-4}	1.69 10^{-7}
A	6.9	1.2	5.39	1.4
ϕ_B (eV)	0.76	0.99	0.73	0.94

TABLE 7.4: Dark diode parameters for heat treated cells.

7.4 JUNCTION CAPACITANCE

The capacitance of CdS/Cu_xS heterojunction has been studied to gain further insight into the nature of the junction. The measurements were made using a phase sensitive detection system at 100 kHz.

First of all the dark junction capacitance-voltage characteristics of type A and type B devices in their as-prepared state were investigated. Plots of C^{-2} versus applied reverse bias generally yielded straight lines indicating the abrupt nature of the junction between CdS and Cu_xS in the as-made condition, (see Fig 7.17). Using the classical interpretation of such plots (see Chapter 3) a net donor concentration (N_D-N_A) of 4.40 10^{15} cm^{-3} was calculated from the slope of this straight line and a diffusion voltage (V_d) of 0.9 V from the intercept on the voltage axis. The depletion region inferred from the conventional formula ($(C/A)_{V=V_o} = \varepsilon\varepsilon_o/W(V_o)$) would therefore be about 0.6 μm. However, as

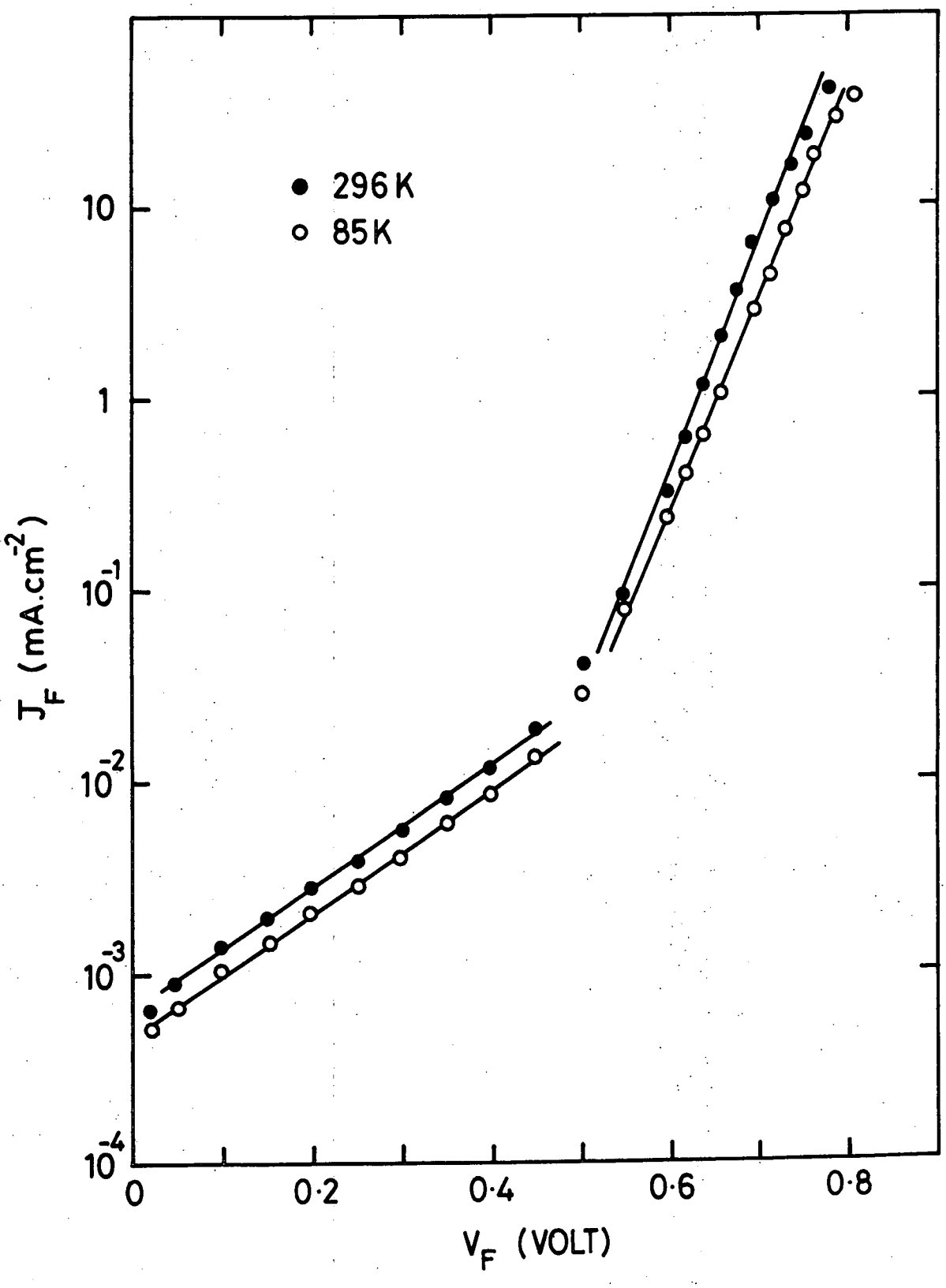

FIG. 7·15 DARK FORWARD J_F / V_F CHARACTERISTICS MEASURED AT 85K AND 296K FOR A TYPE B DEVICE AFTER A TWO MINUTE AIR-BAKE

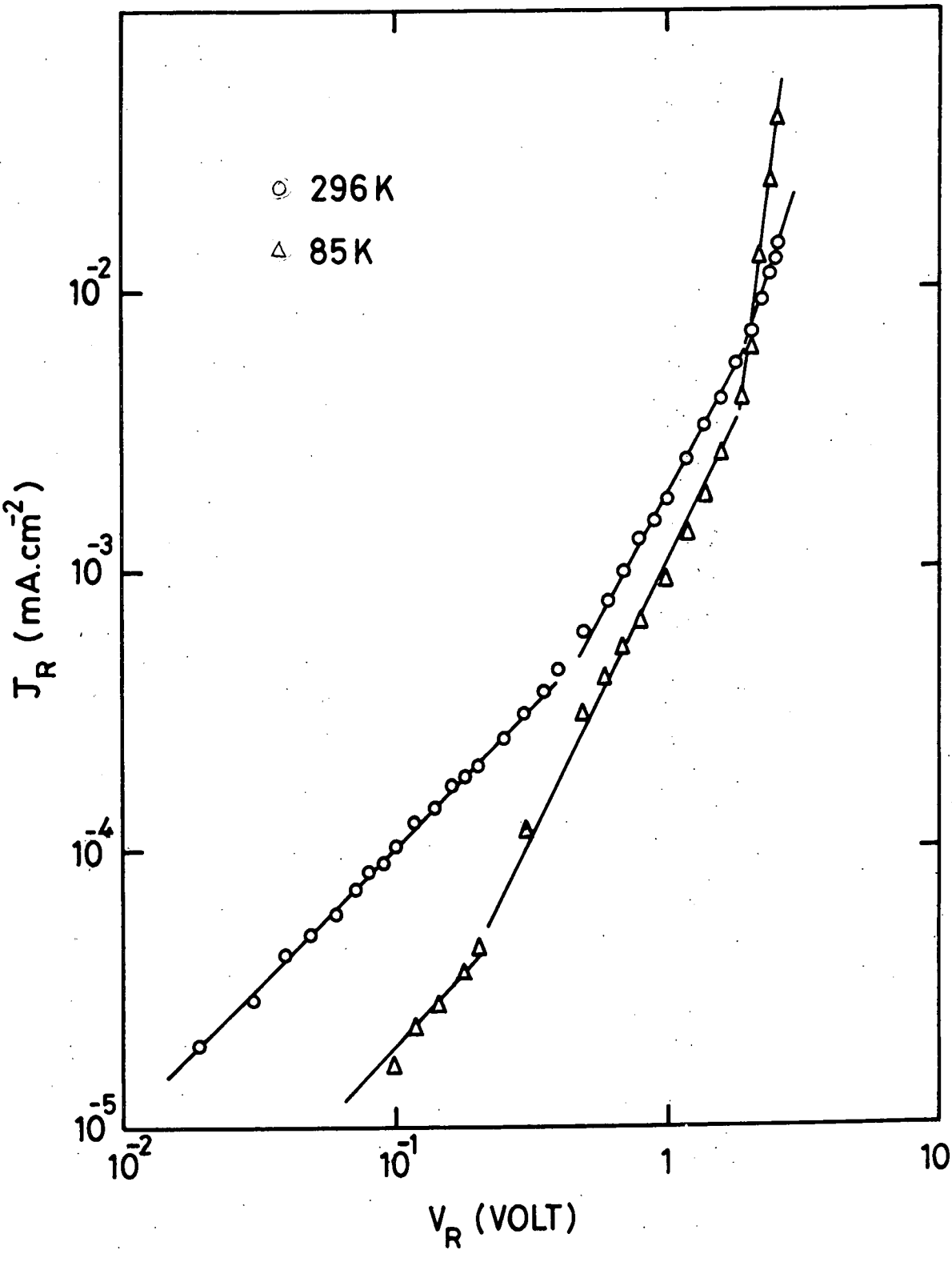

FIG. 7·16 DARK REVERSE J_R / V_R CHARACTERISTICS MEASURED AT 85K AND 296K FOR A TYPE B DEVICE AFTER A TWO MINUTE AIR-BAKE

reported in two previous chapters the actual junction area is considerably larger than the nominal device area and consequently the values inferred from C-V measurements by classical interpretation are not reliable. Furthermore the value of the diffusion voltage is highly dependent on the existence of interface states, dipoles and trapping centres, at or in the vicinity of the junction interface. In fact the intercepts of the C^{-2} vs V plots for as-made cells ranged from 0.3 to 2.5 V, but all the slopes gave almost the same value of N_D-N_A for all samples fabricated on dice from the same crystal boule. Moreover the values of N_D-N_A calculated from simple resistivity measurements assuming that $\mu_n = 300\ cm^2\ V^{-1}\ s^{-1}$ were of the same order of magnitude. The values of the zero bias dark capacitance at room temperature varied significantly from sample to sample from 0.4 nF to 3 nF corresponding to a range of depletion of widths, using nominal areas, from 2.2μm to 0.29μm. This large variation might be partly attributed to an ambiguity as to the real junction area and partly to differences in the junction parameters such as the diffusion potential. A theoretical discussion of junction capacitance and the influence of interface states is discussed briefly in section 3.2 and 3.4.1. However it is not possible to attribute these differences in the capacitance to any specific cause.

The capacitance measurements on type A and type B devices did not reveal any systematic differences between the two types of device as there had been with the J-V and photovoltaic characteristics.

Although junction parameters calculated from C-V measurements are not very reliable, a study of the junction capacitance at different temperatures, before and after heat treatment, was made for comparison purposes. The capacitance at zero bias changes with temperature as shown in Fig 7.18(a). Fig 7.18(b) contains the C^{-2} versus V plots measured at 85 K and 296 K, from which the calculated N_D-N_A values were 4.70×10^{15} and $6.49\ 10^{15}\ cm^{-3}$ respectively. This suggests that the density of positively charged levels

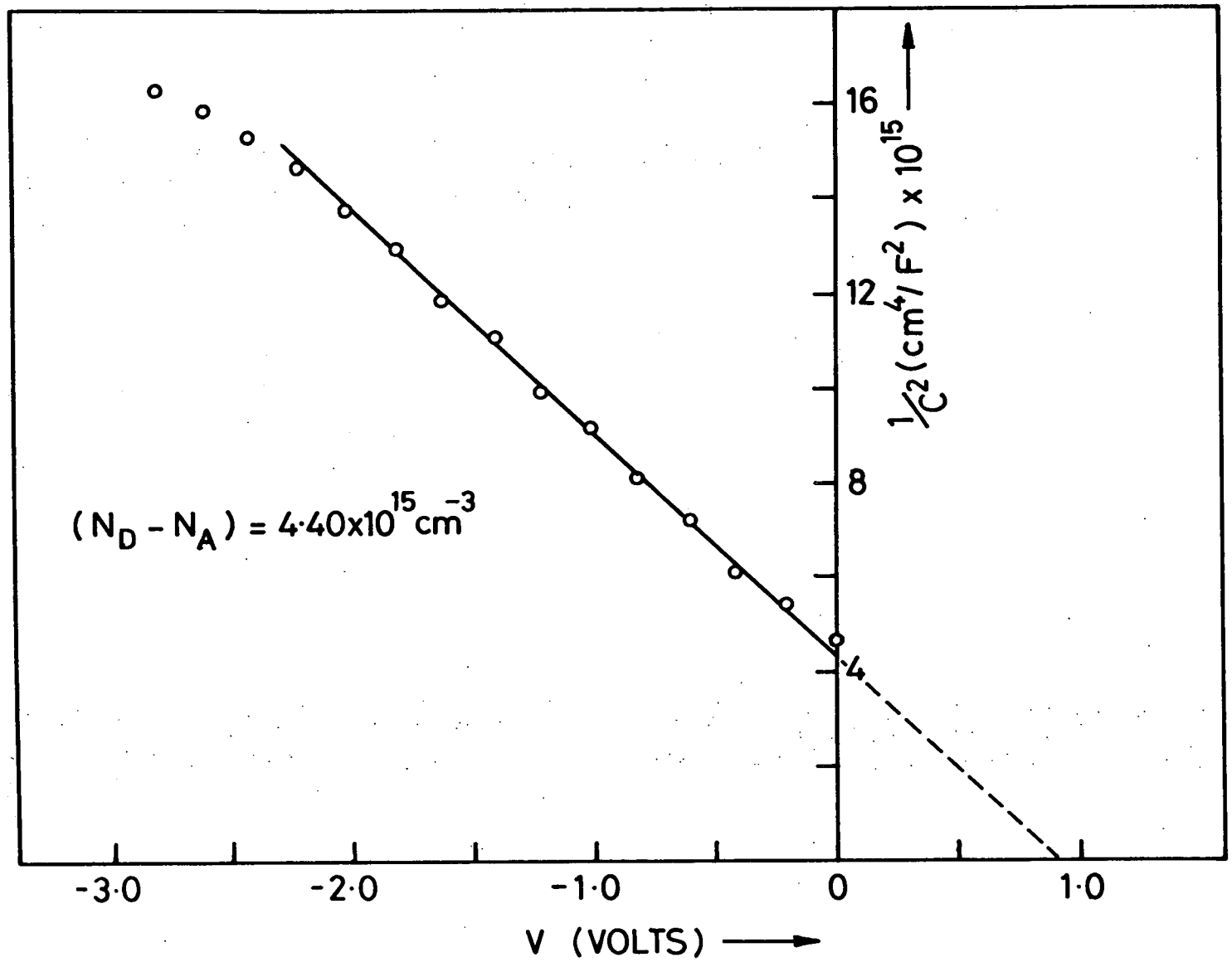

FIG. 7·17 C^{-2} VERSUS VOLTAGE FOR AN AS-MADE TYPE A CELL

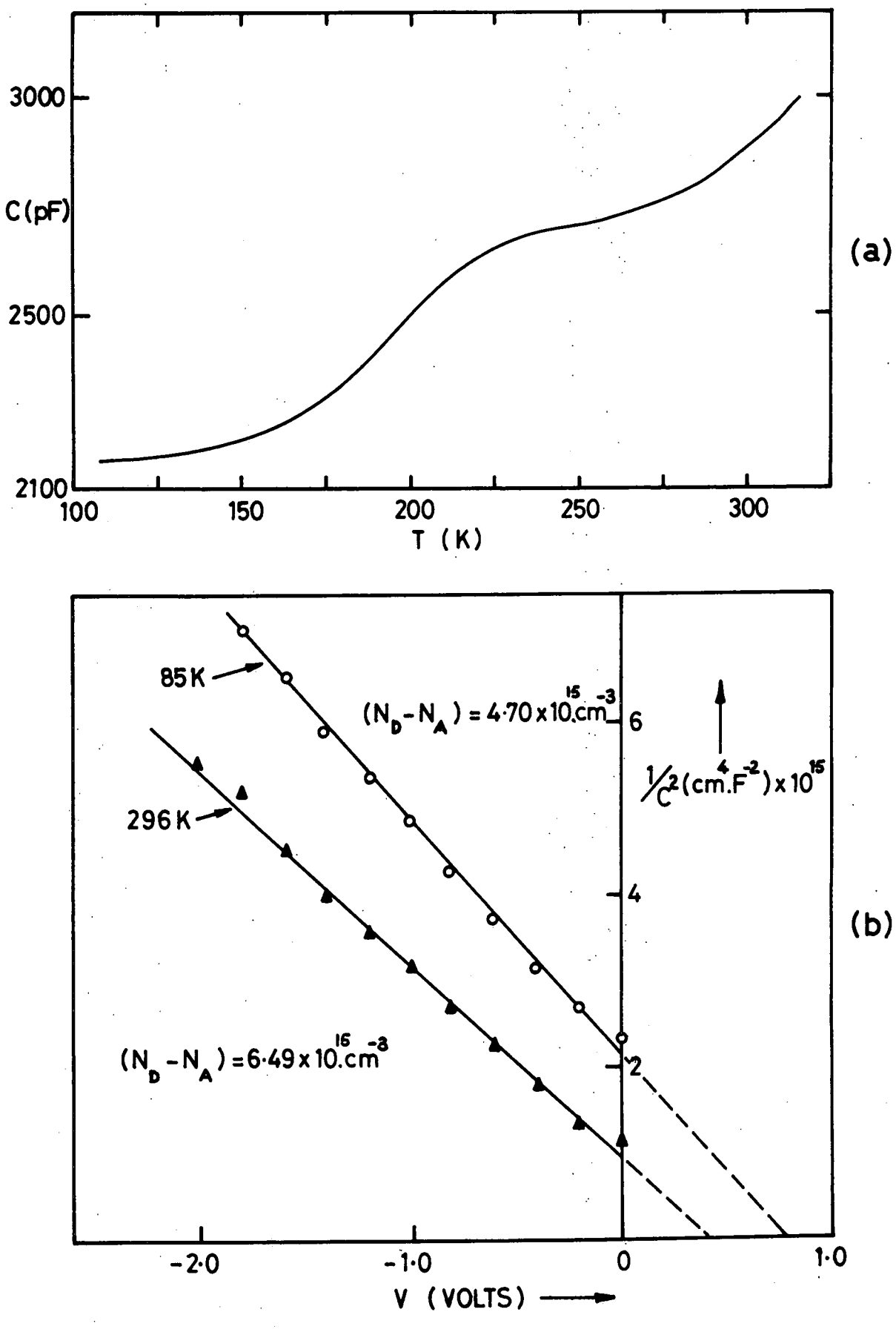

FIG. 7·18 (a) VARIATION OF DARK CAPACITANCE AS A FUNCTION OF TEMPERATURE
(b) C^{-2} / V PLOT AT 296K AND 85K

in the depletion layer had decreased at low temperatures, and the difference in the measured value ($1.79\ 10^{15}\ cm^{-3}$) indicates that the density of levels which can be ionized at room temperature is comparable to the donor density.

The curves in Fig 7.19 demonstrate the effect of a post barrier air-bake on the dark junction capacitance. Linearity of C^{-2} versus V plots allows the estimation of (N_D-N_A) values after different periods of air-baking at 200°C. This particular cell had an N_D-N_A value of $1.77\ 10^{16}\ cm^{-3}$ in the as-prepared state, which was reduced to $8.37\ 10^{15}\ cm^{-3}$ after 1 minute of heat treatment. The dark junction capacitance decreased considerably during the initial 1 minute air-bake, but thereafter the reduction slowed down. After 4 mins air-baking a fifth minute produced virtually no change in capacitance. Different cells reached this condition after varying periods of heat treatment. However, the common feature was that all devices at this stage exhibited a voltage independent capacitance in reverse bias.

Although the junction capacitance of as-made CdS/Cu_2S cells was insensitive to light, it became strongly dependent on the illumination after air-baking. In the following section measurements of photocapacitance and the relation between photocapacitance and photovoltaic sensitivity will be documented.

7.5 PHOTOCAPACITANCE AND INFRARED QUENCHING

In order to explore further the effect of the post-barrier air-bake on the junction properties and to obtain information about the deep acceptor levels introduced by copper diffusion, infrared quenching of photocapacitance was investigated while the device was excited continuously with constant illumination corresponding to the CdS bandgap energy (for details see Chapter 4, 4.7.1). Fig 7.20 demonstrates that after a post barrier air-bake the photocapacitance spectra at room temperature contains two infrared quenching bands. The thresholds of these bands were at 1.75 μm and at 1.13 μm, reaching maxima at 1.36 and at 0.93 μm.

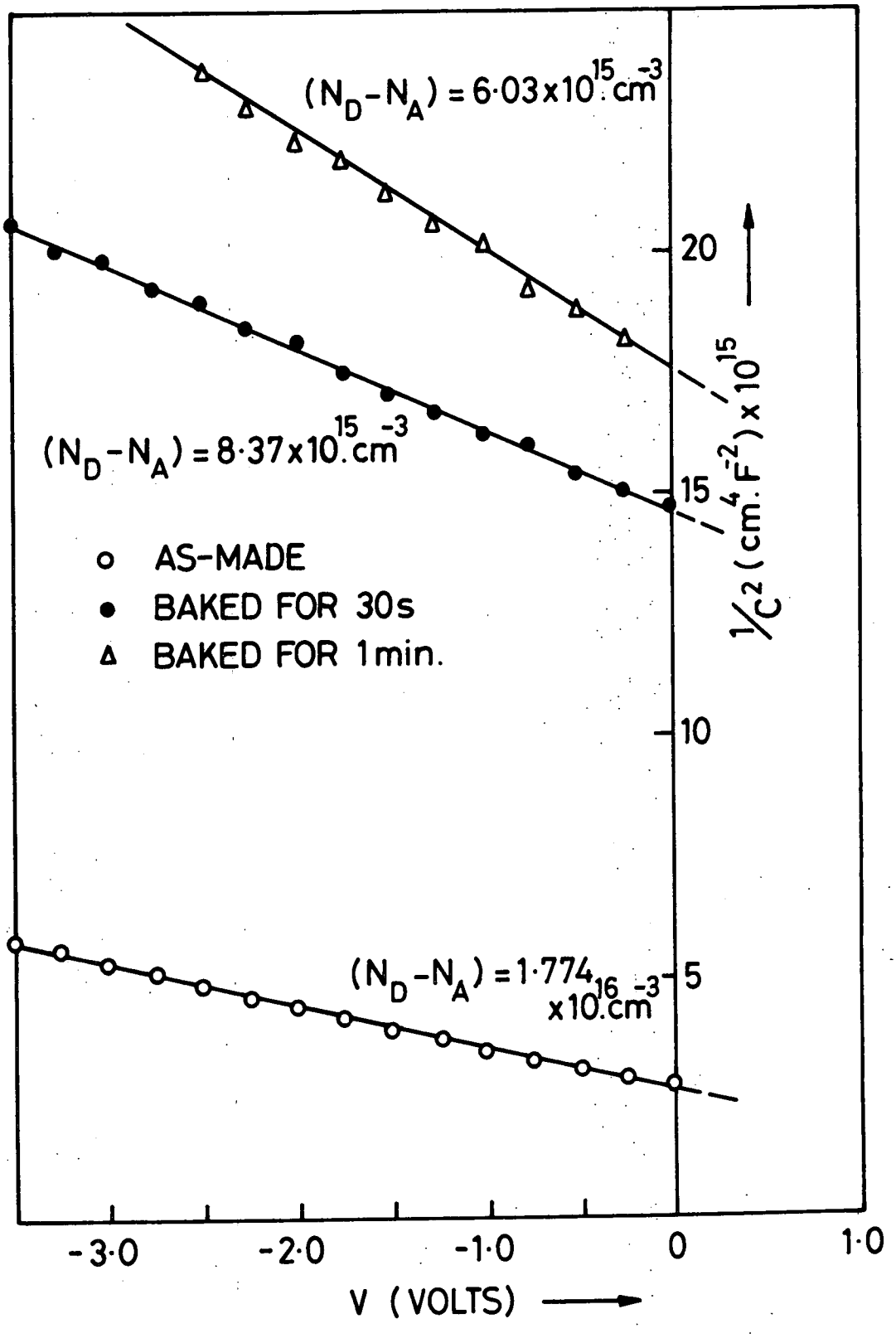

FIG. 7·19 C^{-2} / V PLOTS FOR A CELL GIVEN DIFFERENT PERIODS OF HEAT TREATMENT

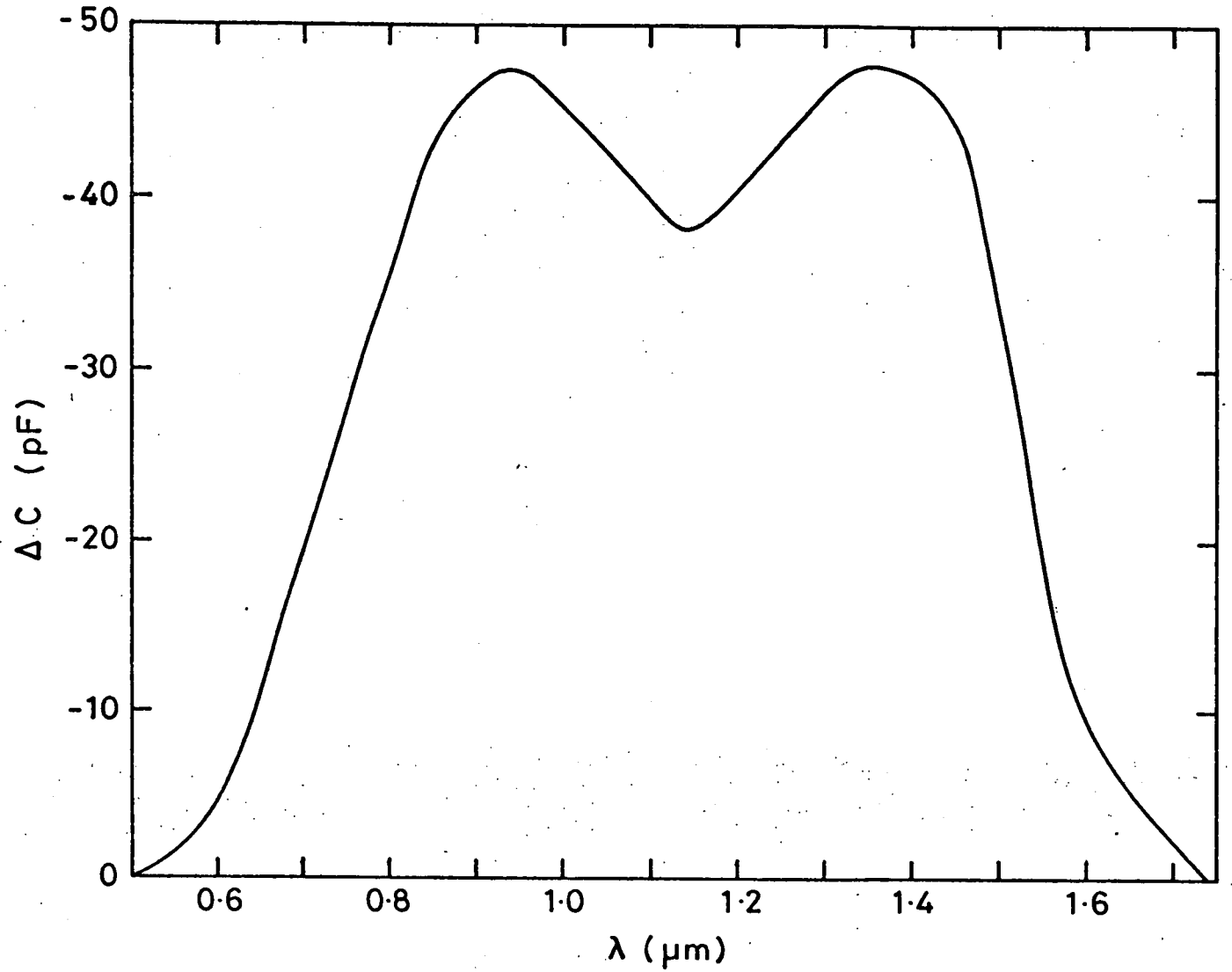

FIG. 7·20 A TYPICAL PHOTOCAPACITANCE SPECTRUM FROM A HEAT TREATED CdS / Cu_2S CELL OBTAINED WITH THE PRECENCE OF 0·52 μm BIAS LIGHT ILLUMINATION

Fig 7.21 shows the spectral responses of the V_{oc} of a cell heat treated for 4 minutes and measured with and without constant bias light illumination. Infrared quenching bands observed in the spectral distributuion of V_{oc} exhibit a similar pattern to those observed in the photocapacitance spectra. However, although the quenching peak at 1.36 μm appeared clearly the second peak at 0.93 μm was not so prominent. This was because this band coincides with the indirect bandgap of the chalcocite phase of Cu_xS.

The other effect of the secondary bias illumination was to enhance the long wavelength response. The relative magnitude of enhancement and quenching was dependent on the intensity of the bias light. The curves in Fig 7.22 demonstrate that after a certain level of the intensity of bias light, which differs from device to device, the quenching bands in the spectral response of V_{oc} become enhancement bands.

7.6 DISCUSSION AND MODELLING OF CdS/Cu_xS HETEROJUNCTIONS

Although a self-consistent theory of the transport of charge carriers in CdS/Cu_2S heterojunctions has not yet been established, it is widely accepted that the current conduction process is a combination of two mechanisms. The first is the thermal excitation of carriers to energies at which the probability of tunnelling into recombination centres is reasonably high ; while the second is the tunnelling recombination of charge carriers via these centres[4,5,6,7,8]. A fairly extensive survey of the proposed models to explain the operation of CdS/Cu_2S cell has been given in Chapter 3, section 3.8. The basic problem of all models suggested is the ambiguity on the interface properties of the junction as the determining factor for the current transport. However recent developments in interface analytical techniques (an elegant review can be found in Ref (9)) are expected to reveal many of the interface parameters accurately in the near future.

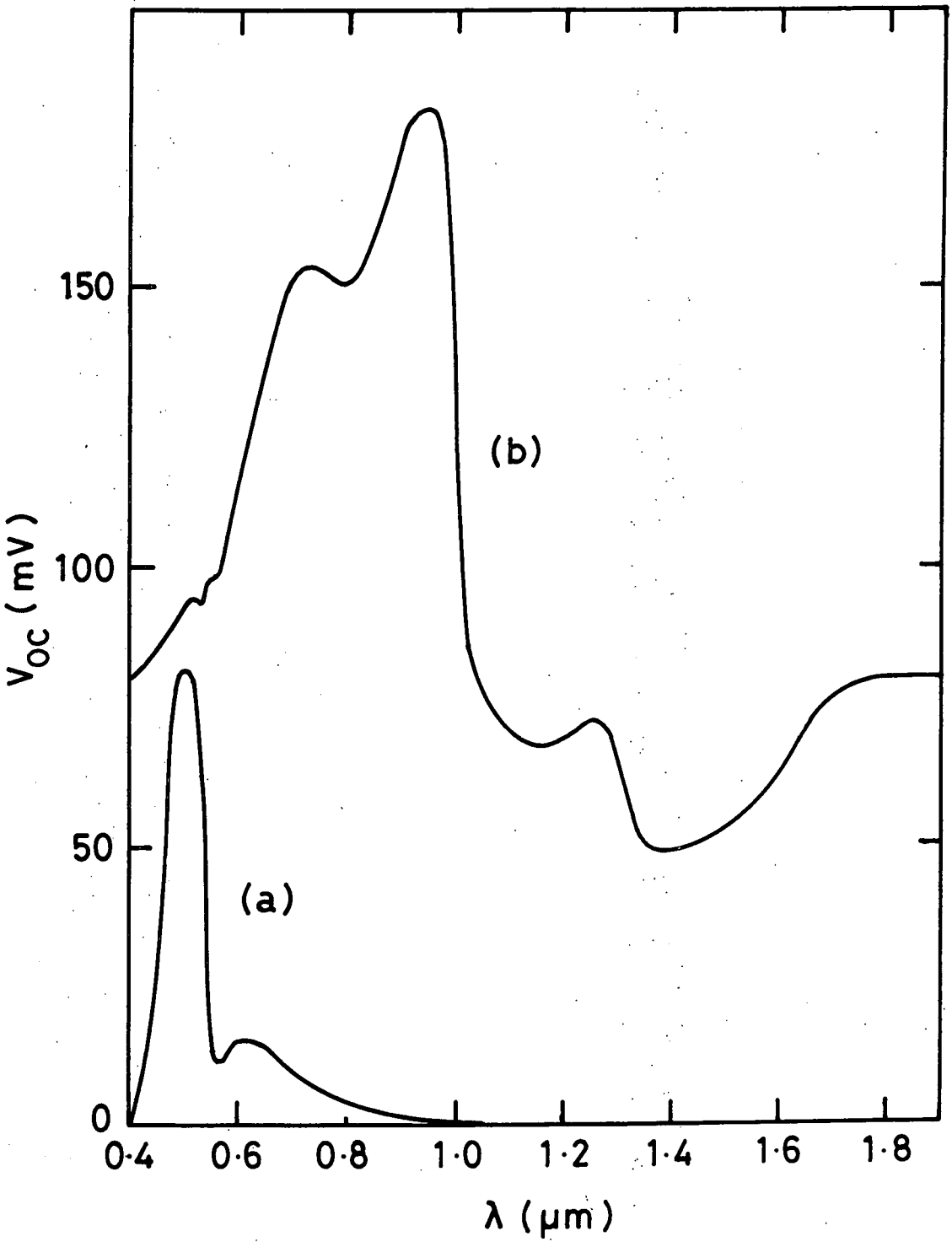

FIG. 7·21 SPECTRAL DISTRIBUTIONS OF V_{OC} FOR A CdS / Cu_xS CELL AFTER 4 MINS. HEAT TREATMENT , (a) WITHOUT BIAS ILLUMINATION, (b) WITH 0·52 μm BIAS LIGHT ILLUMINATION

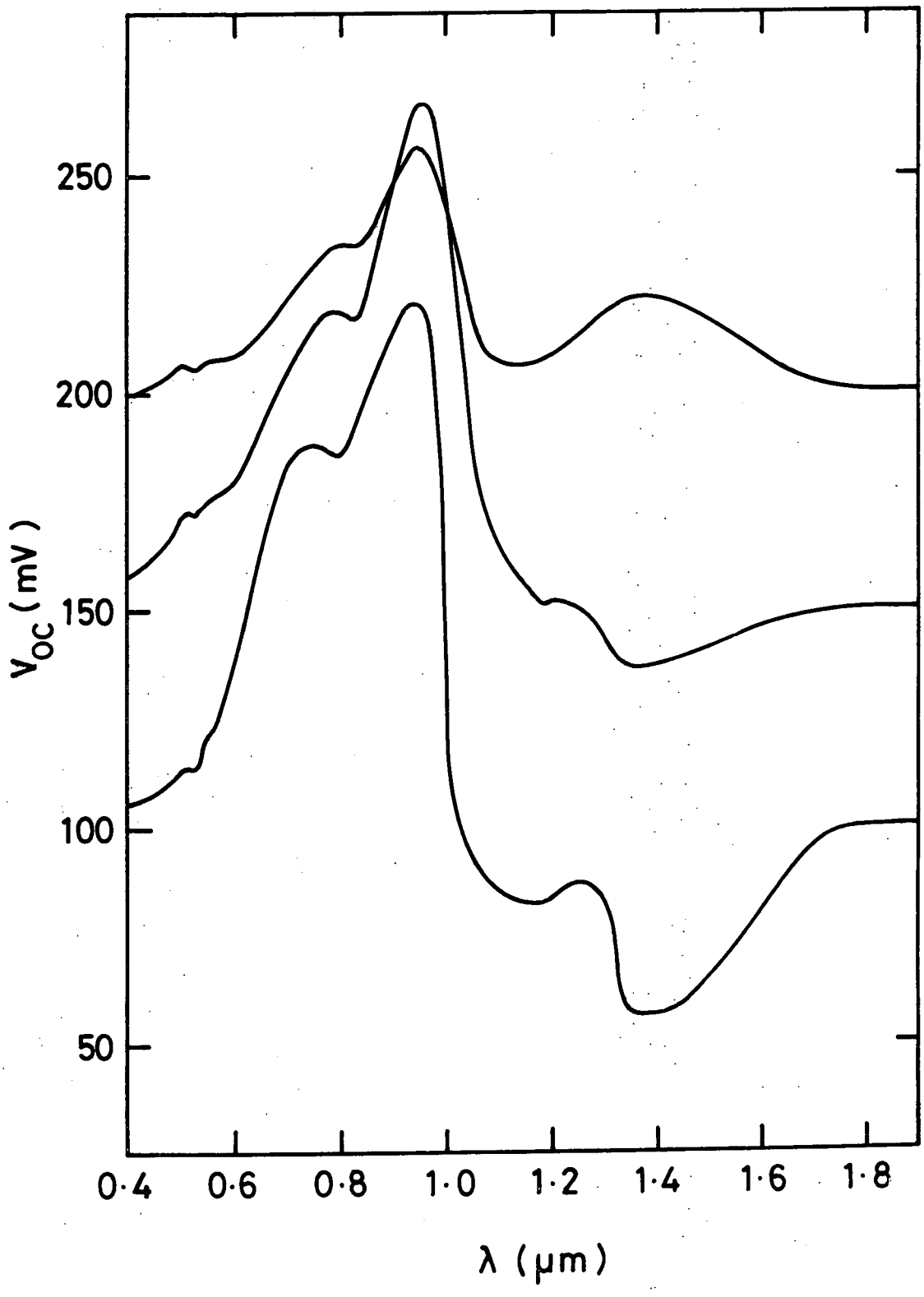

FIG. 7·22 SPECTRAL DISTRIBUTION OF V_{OC} FOR A CdS / Cu_xS CELL AFTER 4 MINS. HEAT TREATMENT FOR DIFFERENT VALUES OF BIAS LIGHT INTENSITY (0·52 μm)

In order to explain the results described in this chapter the band profile of the junction is assumed to be modified during the forming of the junction according to the particular interface that is formed. In fact the bulk electronic properties are thought to be an insufficient guide to determining the discontinuity of the conduction and valence bands. A similar conclusion has been drawn by several researchers, for instance Böer[10] took the chemical and crystallographic nature of the interconnection into consideration, and te Velde[11] suggested variable barrier heights caused by changes in the density of charged interface states. Details of these models are given in Chapter 3, section 3.8. The CdS/Cu_2S cell is a heterojunction diode and because the copper sulphide is degenerate ($p \sim 10^{22}$ cm^{-3}, [6]) and the CdS is non-degenerate ($n \sim 10^{16}$ cm^{-3}) the space charge region occurs entirely in the CdS region. The lattice mismatch of a-parameters of approximately 4.5% between CdS and Cu_xS yields a theoretical interface state density of 5×10^{13} cm^{-2} [12]. Various dark current paths for charge carriers in the heterojunction are summarized in Chapter 3, section 3.4.2 (see Fig 3.2). In general all paths predicted may contribute to the total current crossing the junction. However, depending upon the properties of the interfacial layer, one of the mechanisms dominates the whole current process. Rothwarf[13] suggested that the dominant current path determines the open circuit voltage of the cell. Because many reports concluded that structurally complete cells could exhibit little rectifying behaviour and photovoltaic effect before a post barrier air-bake[4,5,8,11,14,15], all models proposed were basically for heat treated devices. However as is demonstrated clearly in Chapter 5, devices fabricated under optimised conditions give their best performance in the as-made condition. Thus the modelling of the CdS/Cu_2S junction will be evaluated for as-prepared as well as the heat treated samples in what follows. The major characteristics which have to be explained by any suggested model of the as-prepared hetero-

junctions are : (1) the marked differences between the diode characteristics of devices formed on type A and type B surfaces (a) the appearance of three distinct regions in the semilogarithmic plots of the dark forward J-V characteristic of type A devices, and the two regions in type B devices (3) the temperature independent slopes of these plots (except at low voltage) (4) the $J_R = B\ V^{\gamma}$ relationship for reverse currents and the temperature cross-over effect.

These experimental observations may be explained using a multiple diode model in which the junction is assumed to consist of many different quality diodes in parallel, and all mechanisms simultaneously contribute to the diode current. It has already been shown in Chapter 5 that there is a direct correlation between the diode and photovoltaic characteristics of the cells and their surface topography. By microscopic investigation of the surfaces with the EBIC technique, it is concluded in Chapter 6 that the growth of Cu_xS on CdS is complicated in the presence of ledges and kink sites on the hillocks resulting in poorer junction properties, and it is likely that the density of interface states will be higher at these sites. It is therefore suggested that on the microscopic scale local variations of the interface state density will cause a great difference in diode parameters of locally produced barriers.

When the barrier formed on type A surfaces, which is delineated by the array of smoothly facetted hillocks (see Chapter 5 and Fig 5.5), the interface boundary conditions are expected to be fairly similar on the facets of hillocks but the summits and valleys of the hillocks are thought to have quite different interfaces. This is indeed confirmed by the EBIC results described in Chapter 6. Thus, although the interface properties of these differently characterised regions are not known, intuitively it is proposed the smooth sides of the hillocks correspond to good barriers (appearing as light EBIC contrast) whilst the summits and valleys (dark EBIC

contrast) present poor barriers between the CdS and Cu_xS. These are illustrated schematically in Fig 7.23 (a). When the Cu_xS grows on the CdS topotaxially, the lattices are macroscopically connected in a plane perpendicular to c-axis, however on a microscopic scale, most of the interface occurs on planes of higher indices, because of the etched surface topography[16]. In the band diagram shown in Fig 7.23(b), only the interface states caused by the lattice mismatch along the interface plane are considered. These states are positively charged above the Fermi level[17]. At the summits and valleys of hillocks the lattice mismatch and density of interface states is extremely high and the resultant energy band diagram can be represented as in Fig 7.23(c). It is now crucial to understand the recombination path for determining the mechanisms of current flow. When forward bias is applied to the junction, the voltage is distributed unequally among the various diodes with the charge carriers preferentially flowing through the poor diode regions. The total junction area of one specific diode defines the current density which can be transported by the mechanism described. Then, whilst one mechanism approaches saturation as the potential increases, the next conduction mechanism, which gives a better diode characteristic, takes over and so on. The dark forward current voltage characteristics measured for tyep A devices can be explained using this model. The ohmic behaviour in region I is attributed to the tunnelling of charge carriers from the bottom of the CdS conduction band to the interface recombination centres. With voltages up to 0.4 V the second region occurs with a reasonably high current factor and poor diode factor. A slow increase of forward current with applied voltage, in this region, indicates that the current is more sensitive to the density of interface states than to a reduction in the effective barrier height for carrier transport. In fact, the current and diode factors for region II in type A cells, showed large variations from device to device, which can be explained in terms of

the differences in total areas of poor diodes, and in the properties of the interfaces that these barriers contained. The barrier height for the dominant mechanism in region II was varied between 0.45 to 0.61 eV for as-made cells. In region III the value of the diode factor suddenly jumped to high values close to unity (between 1.6 and 2.0). The mechanism which controls the current transport in this region yields a relatively low current factor giving an effective barrier height of about 0.8 eV. Further the direct relation between the level of the current density at which the mechanisms change over, and the ratio of the dark and light EBIC image regions on the total device area confirmed the discussion which was carried out above. Most studies on the current-voltage characteristics of CdS/Cu_2S junctions have shown the existence of three distinct regions in log J_F versus V_F plots[5,8,14,18,19].

To an extent, consideration of the type B surfaces on which kink sites and ledges are numerous, suggests that most of the junction can now be represented by the energy band diagram shown in Fig 7.23(c). The EBIC study of these devices has indeed shown that the dark contrast regions exceed the areas of light contrast. This indicates that the total current capacity of the dark regions at forward bias is very high, and dominates all other mechanisms up to currents of 100 mA/cm^2. In the current controlling regions, transition probabilities of carriers from the bottom of the conduction band of the CdS to the recombination centres is significantly high, because of the very high density of recombination centres per unit area of interface.

In reverse bias a very large barrier opposes hole flow because of large valence band discontinuity ($\sim$ 1.4 eV), so that a high reverse current indicates positively the involvement of tunnelling mechanisms. The investigation of the reverse J-V characteristics of both types of device in their as-prepared states showed that the expression $J \propto BV^{\gamma}$ could be applied

generally with γ taking different values (for instance see Figs 7.2 and 7.10). In type A devices, the reverse and forward current obey the same law ($\gamma = 1$) at low voltages, however at high voltages the reverse current shows a zener current type behaviour with $\gamma = 2$ and 3. With type B devices the reverse current mechanism shows only the J = BV behaviour even at high voltages (up to -4.0 V). This ohmic type of transport indicates that the junctions are shunted by the interface states.

The measurements of the J-V characteristics at different temperatures show that the slopes of the log J_F-V_F plots are virtually independent of temperature confirming the importance of tunnelling (see Figs 7.3, 7.9 and 7.11). The temperature dependence of J_F at fixed voltages for type A cells is clearly different (Fig 7.4) : (i) at low voltages an almost temperature independent current indicates that tunnelling is occurring from the bottom of the conduction band, (ii) at higher forward biases, the current is thermally activated showing that the carriers must be excited to certain energy levels before tunnelling to recombination centres. Activation energy analysis between 85 and 340 K showed that tunnelling occurs with ΔE values of 0.34 eV and 0.6 eV (see Fig 7.6). Unfortunately, the value of the barrier height found from J-V measurements, could not be inferred from activation analysis because of the limitation on the upper temperature which could be used.

In type B devices the weak temperature dependence of the forward current suggests that tunnelling occurs predominantly at energies close to the bottom of the conduction band of the CdS. Thus a very small potential barrier is surmounted before tunnelling (as illustrated in the energy band diagram in Fig 7.23(c)).

The measurements show that the dark reverse currents are not strong functions of temperature for both types of device, giving further confirmation for the tunnelling nature of the current. The reasons for the

cross-over effects observed with reverse currents measured at different temperatures, and the shift in the cross-over point to higher reverse biases, for devices showing good rectification, are not immediately obvious but they may be associated with different charge configurations in the depletion region at different temperatures giving rise to junction electric fields which affect the tunnelling process.

The non-photocapacitive behaviour of the as-made devices may simply be attributed to the absence of copper in the depletion region of the CdS, and linear relation of C^{-2} with reverse biases indicates an abrupt junction. The temperature variation of the capacitance (see Figs 7.18(a) and (b)) may simply be an indication of deep donor like levels (although a detailed study is not attempted in this work DLTS analysis of these devices in our laboratory has shown the existence of 3 discrete electron traps with ionisation energies of 0.18, 0.30, and 0.38 eV). The presence of large densities of deep donor like levels in CdS which appears to be a result of junction formation[8] gives rise to a much more abrupt band profile at the interface than that expected for the shallow donor density of the bulk. Although the donor concentration indicates that the tunnelling probabilities from the conduction band of the CdS into interface states are fairly small, these deep donor levels increase the tunnelling probabilities considerably by narrowing the tunnelling distance and increasing the electric fields near the interface.

To summarise therefore the experimental observations on as-made CdS/Cu_2S devices can be explained in terms of a model (Fig 7.23 (a,b,c,d) incorporating the following features :

(1) The junction consists of many different regions with different parameters (mainly connected with differences in the density of interface recombination centres).

(2) The energy band profile of these regions is determined during the forming of the junction according to the particular interface that is formed.

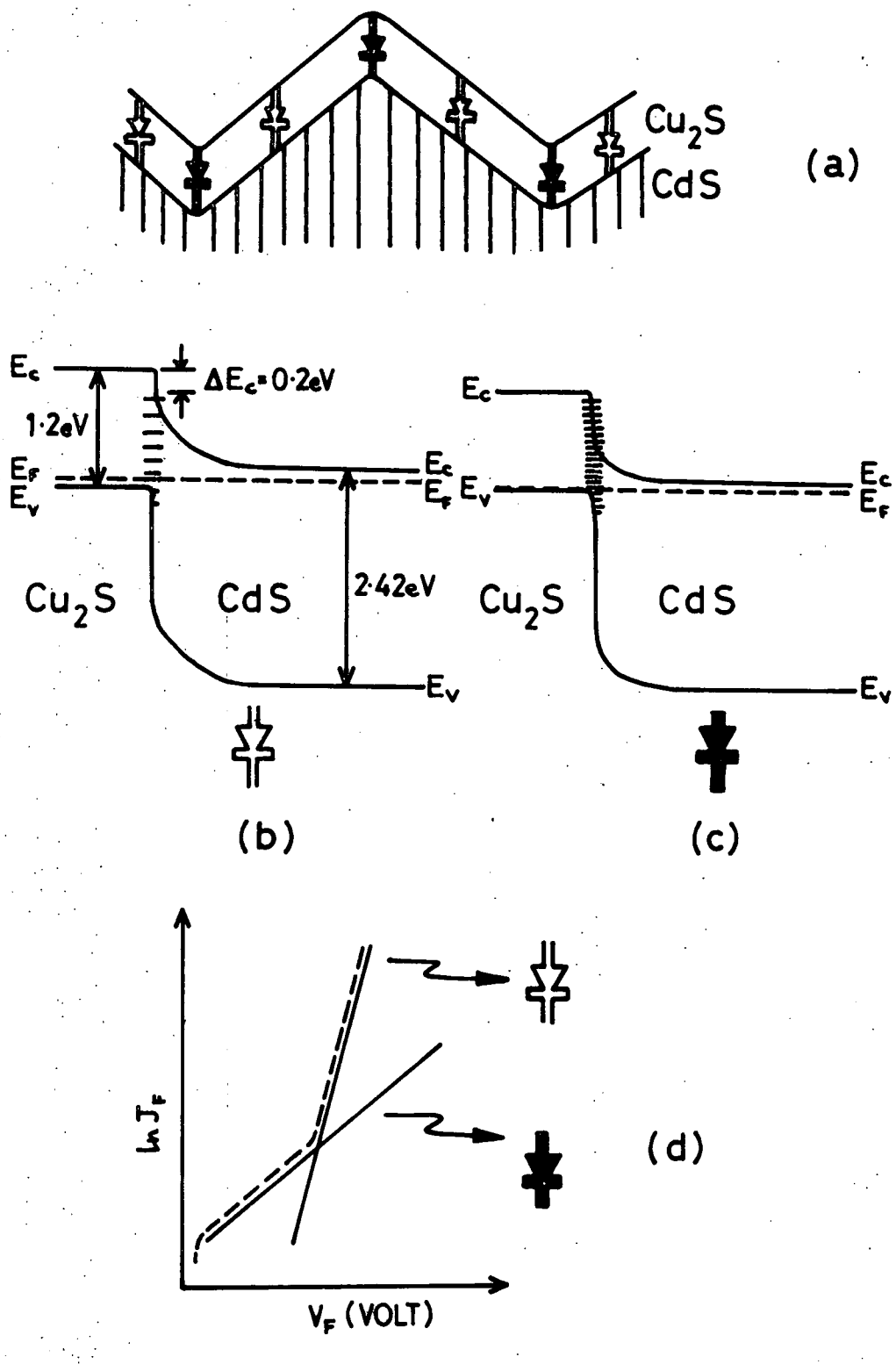

FIG. 7·23 PROPOSED MODEL TO ACCOUNT FOR THE OBSERVED VARIATION IN CELL PERFORMANCE WITH SURFACE TOPOGRAPHY.

(a) Schematic diagram of junction cross-section at a hillock.

(b) & (c) Band diagram for a region with low (b) and high (c) interface state density

(d) Association of the regions of the surface giving rise to different performance with the different regions of the dark diode characteristics.

(3) The mechanism for dark forward-bias current flow is thermally activated tunnelling -recombination via interface recombination centres, and the activation energy of the tunnelling process varies from region to region depending on the junction interface. Tunnelling recombination currents from different activation energies contribute to the diode current simultaneously.

(4) The proportion of the regions with good parameters relative to those with poor parameters determine the ultimate behaviour of the cell.

The measurements made on cells suggested that an air-bake can be explained by invoking the same key features discussed in Chapter 5. Firstly the heat treatment causes oxygen to be absorbed at the junction interface where it forms electron traps[11], this results in an increase in barrier height. Some authors propose that the absorbed oxygen produces a thin interfacial layer ($\sim$ 10 Å) between the CdS and the Cu_xS[20,21]. Further, it is widely recognized that copper diffuses from the Cu_xS into the CdS compensating the CdS near the junction interface during the air-bake (All references on CdS/Cu_xS cells).

The presence of acceptor impurities widens the depletion region in the dark and may compensate the deep donor like levels, so that the tunnelling processes responsible for forward current with the low activation energies are dramatically reduced. The onset of photocapacitance quenching bands at 0.71 eV and 1.09 eV and their maxima at 0.91 eV and 1.33 eV can be interpreted as the combined effects of copper levels located at 0.3 eV above the valence band and at the vicinity of the midband gap (1.1-1.2 eV) as has been reported by many workers on this line[4,8,22,23,24].

Rothwarf[13] reported that the copper compensation reduces the net donor density by three orders of magnitude. When the heat treatment is prolonged the width of the compensated layer exceeds the space charge region so that a high resistivity CdS region exists between the end of depletion layer and the uncompensated CdS region. The suggested energy band diagram

for a heat treated CdS/Cu_xS heterojunction is shown in Fig 7.24. This model is similar in many respects to that suggested by the Delaware group. The high forward voltages used in the forward characteristics of heat treated cells can be explained by negative charge storage in the compensated region in the bulk. Nevertheless, when the junction is illuminated with light with sufficient photon energy to excite electrons from the acceptor levels to the conduction band the depletion width narrows towards its as-made value. It might be thought that the diode characteristic would also return to its as-prepared state under sufficient illumination but this is not so. The hard diode characteristics of heat treated type B cells under illumination suggest that the absorbed oxygen at the interface plays the main role in the improvement of the diode characteristics. The model suggested here for the heat treated cells can explain all the experimental observations. Indeed the C^{-2} versus V_R plots in Fig 7.19 demonstrate the progressive compensation of the CdS, and the high voltage forward bias region of the dark J-V characteristics confirms the existence of the resistive region. Further, the rather similar junction properties achieved for both types of device after heat treatment (see Table 7.4) indicate that the formation of oxygen traps stems the tunnelling process at lower activation energies, so that conduction occurs by tunnelling recombination at high energies in both types of device.

The model can also explain the spectral response of heat treated devices and the effect of bias light on the spectral distribution of the photovoltaic response. As stated in Chapter 5 the photoresponse of an unbaked cell was essentially that of Cu_xS. However, the spectral response of heat treated cells is strongly influenced by the intensity and wavelength of the light reaching the CdS. The reduction in the long wavelength response can be partly explained by the shift of the Cu_xS response to shorter wavelengths with heat treatment, and partly attributed to the insufficient energy of photons to ionise all deep acceptors for energies smaller than 1.3 eV (see Chapter 5, Fig 5.29). The incident photons with energies greater than

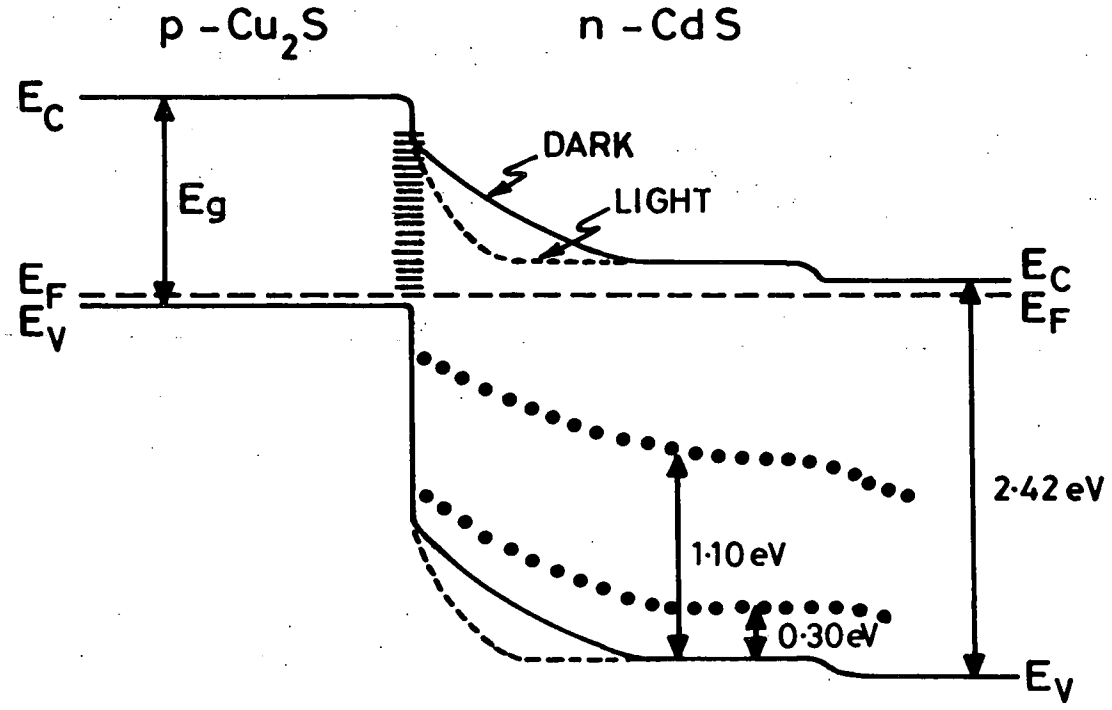

FIG. 7·24 ENERGY BAND DIAGRAM OF HEAT TREATED CdS / Cu_xS CELL ILLUSTRATING THE COMPENSATED REGION OF CdS LAYER AND THE LIGHT INDUCED CHANGE IN THE BAND DIAGRAM

1.3 eV ionise the copper acceptor levels and cause a jump in the junction field to higher values, and reduction in the resistance of the compensated layer, so that the interface collection factor depends strongly on the illumination. Although irradiation of some wavelengths may increase the positive charge density in the space charge region by ionising deep levels, other wavelengths could result in the filling of these levels. The spectral response of a baked cell is determined by the rate and the sequence in which the wavelengthis scanned.When a junction was excited continuously with light corresponding to the CdS bandgap, all levels were assumed to be ionised, with the depletion region shrinking back to its as-prepared value. The change in the depletion region caused by the irradiation is shown by the dashed line in Fig 7.24. If the junction is then scanned with monochromatic light from the infrared to shorter wavelengths the levels at 0.3 eV and the mid bandgap will be refilled and the electric field at the junction will decrease towards the dark condition. Then the photovoltaic effect created by the bandgap illumination will be quenched significantly at 1.36 μm (see Fig 7.21). However, the expected quenching at 0.91 μm competes with the chalcocite response and the quenching at this wavelength does not appear as clearly as it does in the photocapacitance. The competition between quenching and enhancement shows a close relation with the light intensity. As the secondary light intensity increases the response at about 0.96 μm increases and the magnitude of the quenching peak decreases. In fact after a certain level of intensity the infrared quenching bands become enhancement bands (see Fig 7.22). In order to establish positively the correlation between the observed spectral response and the deep levels in the CdS bandgap, the density, location distribution and capture cross-sections of these levels have to be known. However, although a vast number of reports are available describing levels in the CdS bandgap[4,8,13,23,24], no complete set of data for any level has definitely been established. Thus any further discussion of the modification of the energy band diagram by the type of illumination can only be speculative.

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CHAPTER 8

SINGLE CRYSTAL $Zn_xCd_{1-x}S/Cu_2S$ PHOTOVOLTAIC CELLS

8.1 INTRODUCTION

With the present technology the efficiency of CdS/Cu_2S thin film photovoltaic cells is estimated to be limited to about 10%[1] because of differences in the electron affinities and the lattice spacings of the two semiconductors from which the heterojunction is formed. One way of improving the matches between the crystal lattices and the electron affinities is to incorporate zinc into the CdS to form a solid solution of $Zn_xCd_{1-x}S$ as first suggested by Palz et al[2]. Recently thin film cells based on $Zn_xCd_{1-x}S$ have been produced with an efficiency of up to 10.2%[3]. However, this is far from the upper limit which is estimated to be about 14-15%[1]. The discrepancy between the best experimental efficiency and the estimated limiting value is under continuous investigation throughout the world.

In this chapter results are presented for $Zn_xCd_{1-x}S/Cu_2S$ photovoltaic cells which have been prepared on single crystal substrates of $Zn_xCd_{1-x}S$ with compositions in the range $0<x<0.4$. The characterisation of $Zn_xCd_{1-x}S$ crystals, the determination of their lattice parameters and the surface preparation prior to the formation of the copper sulphide layer are described in section 8.2. The following section is devoted to an examination of the local photovoltaic sensitivity of $Zn_xCd_{1-x}S/Cu_2S$ cells, using the electron beam induced current (EBIC) technique and its correlation with cell performance under 100 mW/cm^2 illumination. The copper sulphide layer and the photovoltaic spectral responses of these cells are described in section 8.4. The dark current voltage measurements and the study of junction capacitance are presented in sections 8.5 and 8.6 respectively.

In order to avoid confusion, the copper deficient phases of copper sulphide are referred to in this chapter as Cu_yS where y replaces the x used in the earlier chapters.

8.2 STRUCTURE AND SURFACE PREPARATION OF $Zn_xCd_{1-x}S$ SINGLE CRYSTALS GROWN FROM THE VAPOUR PHASE

The technique employed to grow large single crystals of $Zn_xCd_{1-x}S$ utilised the vapour phase technique, details of which have already been given in Chapter 4, section 4.2. With this method satisfactory homogeneous crystal boules were obtained for all crystals with Zn compositions up to $Zn_{0.3}Cd_{0.7}S$. With higher zinc concentration there was some evidence that the growth of uniform mixed crystals was limited and a colour gradation along the length of the boules became apparent. A few attempts were made to determine the composition of $Zn_xCd_{1-x}S$ crystals by means of atomic absorption spectroscopy of samples dissolved in concentrated HCl. The results indicated that when a $Zn_xCd_{1-x}S$ single crystal is dissolved in HCl, some of the zinc precipitates out and although the measured value of the cadmium content agreed with the expected value, the measured level of Zn was always found to be far too low. Thus the values of the bandgap measured optically had to be used to monitor the compositions.

The crystal structure of boules with $0 \leq x \leq 0.5$ was hexagonal, and the x-ray powder photography technique was used to determine the variation of the lattice parameter with composition. The values of the planar spacings were determined from the x-ray pattern and then indexed using the CdS plane spacing as standard (ASTM), see section 4.2.1 for details. The results of these measurements are illustrated in Fig 8.1 which shows that both a_o and c_o decreased sublinearly with increasing zinc content.

To ensure that the results obtained using single crystal material might bear some relation to thin films all devices were prepared on etched

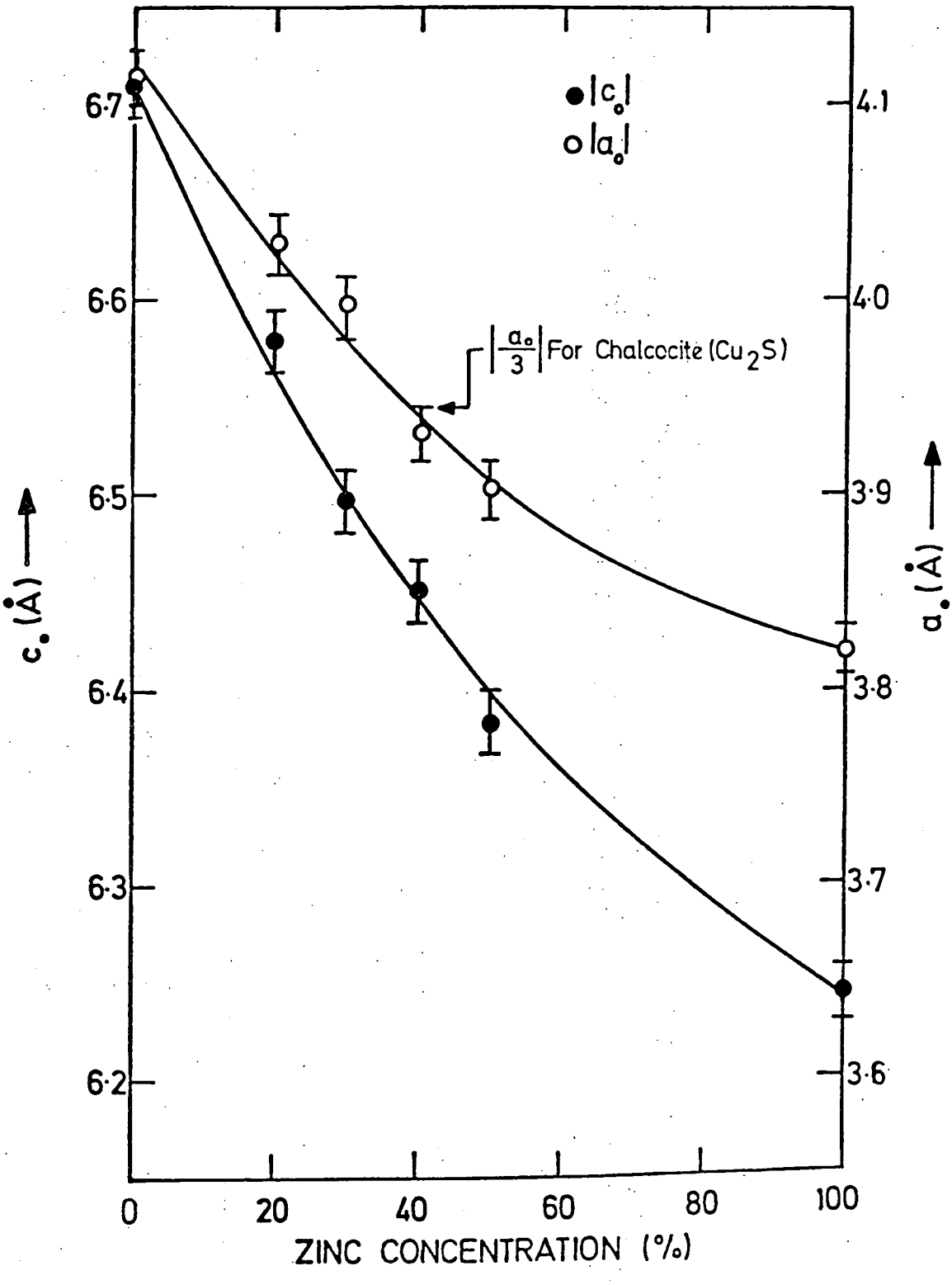


FIG. 8·1 VARIATION OF LATTICE PARAMETERS WITH COMPOSITION OF $Zn_x Cd_{1-x}S$ CRYSTALS

$(000\bar{1})$ faces of the $Zn_xCd_{1-x}S$ single crystals, as this orientation corresponds to the preferred orientation of the grains in thin films. Consequently all crystals were aligned using X-ray back reflection. Then dice with dimensions of 4 x 4 x 2 mm^3 were cut from the boules so that the largest area faces of each die coincided with the basal plane of the hexagonal structure. As discussed in Chapter 5 for CdS, the final stage in removing the severe saw marks arising from cutting was to polish the large area faces mechanically with 1 μm alumina powder. RED examination of such surfaces indicated that the polishing created polycrystalline layers on the $Zn_xCd_{1-x}S$ single crystals. RED patterns of these polycrystalline layers for each composition, $0 \lesssim 0 \lesssim 0.4$ were indexed as arising from a totally sphalarite cubic structure. Fig 8.2 shows a RED pattern for $Zn_{0.3}Cd_{0.7}S$ with a lattice parameter of 5.80 Å. To remove this layer, which is neither suitable for device fabrication nor representative of thin film material, all dice were etched in cold concentrated HCl for a period of 30s. As with CdS (section 5.2) the sequence of cutting and polishing also had a considerable effect on the ultimate topography of an etched $(000\bar{1})$ surface of a $Zn_xCd_{1-x}S$ crystal. For instance, the surface of an etched die which had been polished as a slice before being cut into dice, gave rise to the type of surface shown in Fig 5.5 (type A), while the surfaces of dice which had been polished after cutting into dice were similar to that depicted in Fig 5.6 (type B). Because of the close similarities between the surface preparation of CdS and $Zn_xCd_{1-x}S$ and the resultant secondary emission micrographs these details are omitted here, but the effects are entirely similar to those described in section 5.2.

The electrical conductivity of the crystals at room temperature as a function of composition $(0 \lesssim x \lesssim 0.4)$ ranged from 0.5 to 2 $\Omega^{-1}\ cm^{-1}$ and was independent of illumination.

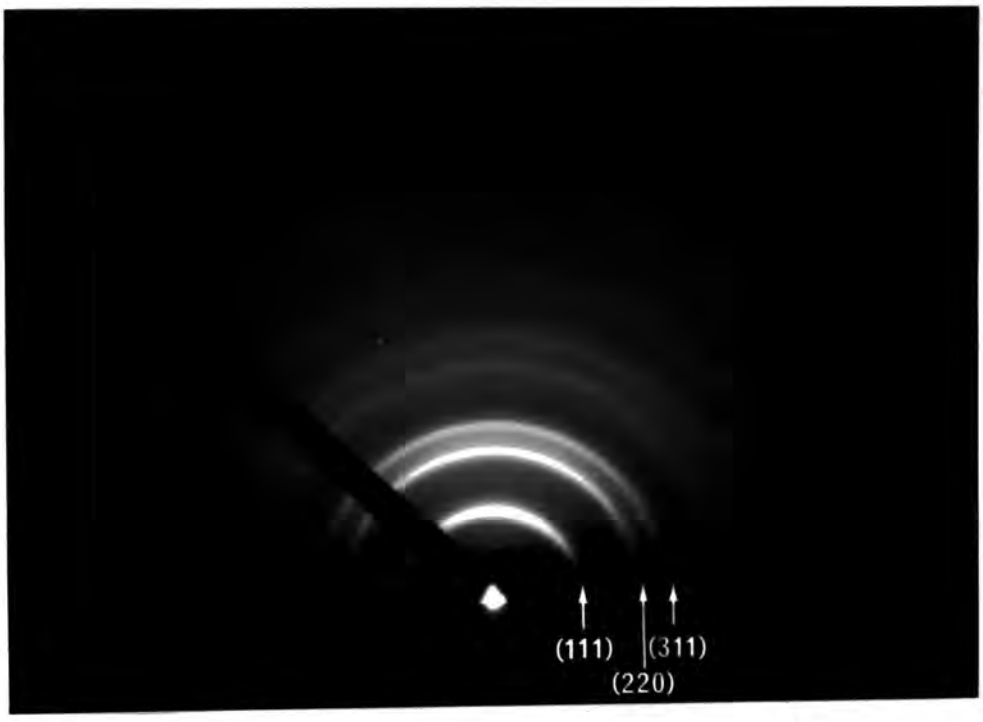


Figure 8.2 : Reflection electron diffraction pattern from the polished surface of a $Zn_{0.3}Cd_{0.7}S$ crystal.

8.3 STUDY OF LOCAL PHOTOVOLTAIC SENSITIVITY USING THE EBIC TECHNIQUE

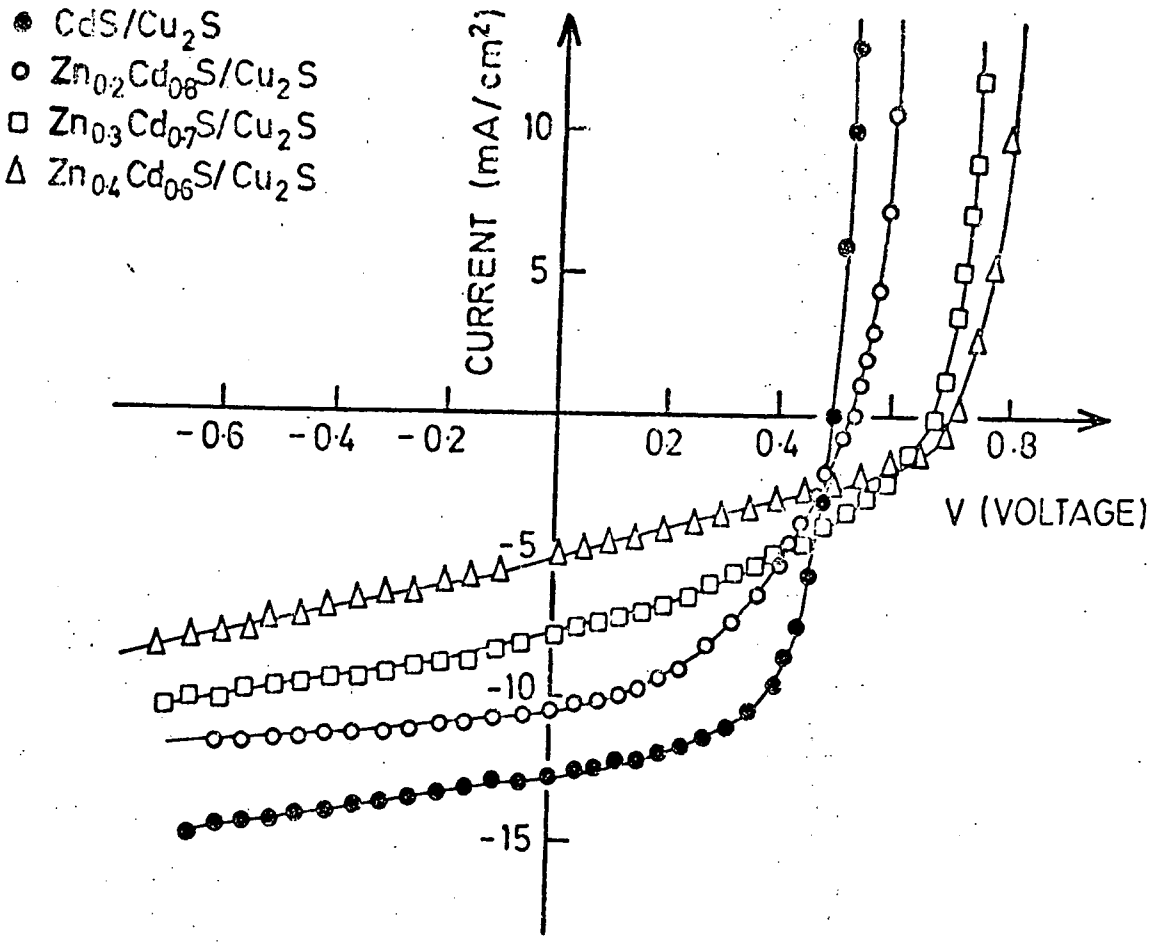
In the preparation of devices an indium ohmic contact was applied to the Cd face of all dice, and the topotaxial layer of copper sulphide was grown at 95°C on to the opposite freshly etched sulphur faces by dipping in the plating solution for 10s. Details of this process are given in Chapter 5, section 5.3. An evaporated 1 μm diameter Au contact was deposited on the copper sulphide for the second electrode. No loss minimisation processes were employed.

When devices were fabricated on the surfaces which featured numerous kink sites on etched hillocks (type B), EBIC examination confirmed that the local photovoltaic sensitivity of the surface was poor (dark EBIC image) in the regions where numerous kink sites and ledges occurred. Indeed, as with CdS based cells, devices made on type B surfaces consistently exhibited poor diode and photovoltaic behaviour due to the presence of large numbers of kink sites and ledges. This clear relation between surface features and the EBIC image may be seen by comparing Figs 6.7 and 6.8 in Chapter 6 (in order to avoid needless repetition similar SE and EBIC micrographs for $Zn_xCd_{1-x}S/Cu_2S$ are not reproduced here).

Since our primary interest is in high efficiency devices, all characteristics described in this chapter are for cells fabricated on type A surfaces. This type of surface gave rise to an EBIC image similar to that depicted in Fig 6.6 for CdS/Cu_2S.

8.3.1 Cell Performance

Typical current-voltage characteristics measured under AM1 illumination for as-made devices prepared on substrates in which the zinc content ranged from x = o to x = 0.4 are shown in Fig 8.3. The values of V_{oc} and J_{sc} averaged over four devices prepared for each substrate composition are recorded in Table 8.1. The properties of these cells can be summarised as follows :



	CdS/Cu_2S	$Zn_{0.2}Cd_{0.8}S/Cu_2S$	$Zn_{0.3}Cd_{0.7}S/Cu_2S$	$Zn_{0.4}Cd_{0.6}S/Cu_2S$
OCV (VOLT)	0·499	0·548	0·681	0·726
SCC (mA/cm^2)	12·75	10·36	7·71	4·99

FIG. 8·3. CURRENT–VOLTAGE CHARACTERISTICS AS-MADE FOR $Zn_X Cd_{1-X} S/Cu_2S$ CELLS MEASURED UNDER 100mW cm^{-2} ILLUMINATION.

(i) V_{oc} increased from 500 mV with CdS to 720 mV with $Zn_{0.4}Cd_{0.6}S$.

(ii) Higher V_{oc} values were accompanied by a decrease in the values of J_{sc} and fill factor from 12.75 mA cm^{-2} and 0.65 with CdS to 4.99 mA cm^{-2} and 0.35 with $Zn_{0.4}Cd_{0.6}S$.

(iii) As a result of (ii) the efficiencies of all mixed crystal cells were less than those of the CdS devices.

TABLE 8.1 : The values of V_{oc} and J_{sc} averaged over four devices prepared for each of the substrates compositions.

	$CdS-Cu_2S$	$Zn_{0.2}Cd_{0.8}S-Cu_2S$	$Zn_{0.3}Cd_{0.7}S-Cu_2S$	$Zn_{0.4}Cd_{0.6}S-Cu_2S$
V_{oc} (volts)	0.50	0.55	0.68	0.72
J_{sc} (mA cm^{-2})	12.75	10.36	7.71	4.99

The current-voltage characteristics for as-prepared devices with a range of Zn compositions up to 40 molar percent, measured under AM1 illumination and in the dark, converged towards each other in forward bias, but did not cross-over. Also, as with CdS based cells, reverse bias characteristics under illumination are simply equivalent to the downward displacement of the dark reverse characteristic by an amount equal to the short circuit current. Because of the increasing difficulty of growing uniform boules with high zinc concentrations the device study has not been extended to substrates containing more than 40% molar of zinc.

Interestingly, no device fabricated on $Zn_xCd_{1-x}S$ single crystals could be improved by a post barrier air-bake, although the dark reverse current was reduced, and there was a small increase in V_{oc} and fill factor.

The value of J_{sc} decreased considerably after a 2 mins air-bake at 200°C. Once again, because the variation in the properties of $Zn_xCd_{1-x}S$ cells are similar to those of CdS ones, results are not presented in detail and are similar to those in Chapter 5, section 5.6.1.

8.4 THE COPPER SULPHIDE LAYER AND SPECTRAL RESPONSE

Reflection electron diffraction studies of copper sulphide layers formed on the sulphur planes of the mixed crystals confirmed that the amount of djurleite that existed in these layers increased with increasing zinc content. With the devices formed on $Zn_{0.4}Cd_{0.6}S$ substrates, the mixture of chalcocite and djurleite was dominated by djurleite. RED patterns for chalcocite and a chalcocite-djurleite mixture are shown in Chapter 5, Fig 5.11 and Fig 5.14 respectively. SEM examination of the cleaved cross-sections of $Zn_xCd_{1-x}S$ heterojunction indicated that the copper sulphide layers were thinner when the zinc content was larger.

The spectral response curves of V_{oc} and J_{sc} for an as-made cell on a substrate of $Zn_{0.3}Cd_{0.7}S$ are shown in Fig 8.4. The curves have not been corrected for the variation in energy of the light emerging from the exit slit of monochromator, which is consequently shown separately in the same figure. Both response curves show three peaks at 0.96, 0.70 and 0.46 μm. It has already been established in Chapter 5 that the two longer wavelength bands correspond to the absorption of light across the indirect bandgap of chalcocite ($\sim$ 0.96 μm) and the direct bandgap of djurleite (0.7 μm). The small peak at 0.46 μm represents the photovoltaic response accompanying light absorption in the underlying $Zn_{0.3}Cd_{0.7}S$. As is obvious from Fig 8.4 the shapes of the V_{oc} and J_{sc} curves are very similar.

The relative spectral response curves of V_{oc} for some as-prepared devices on crystals of different compositions are illustrated in Fig 8.5. These curves confirm that the magnitude of V_{oc} increases with increasing zinc content, and that there are two major bands at the same wavelengths,

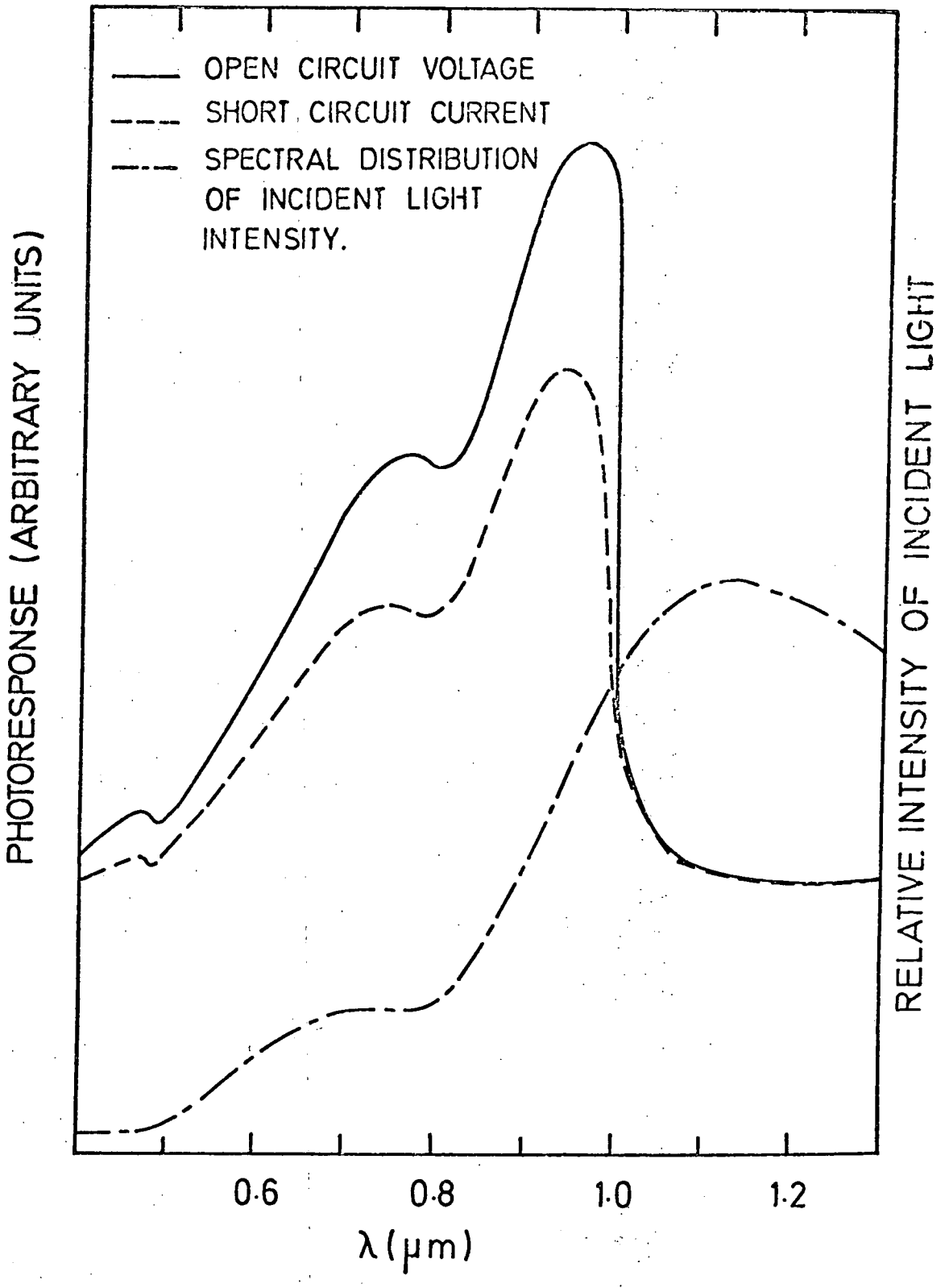


FIG.8·4. SPECTRAL RESPONSE OF OPEN CIRCUIT VOLTAGE AND SHORT CIRCUIT CURRENT AT ROOM TEMPERATURE FOR AS-MADE $Zn_{0.3}Cd_{0.7}S/Cu_2S$ CELL.

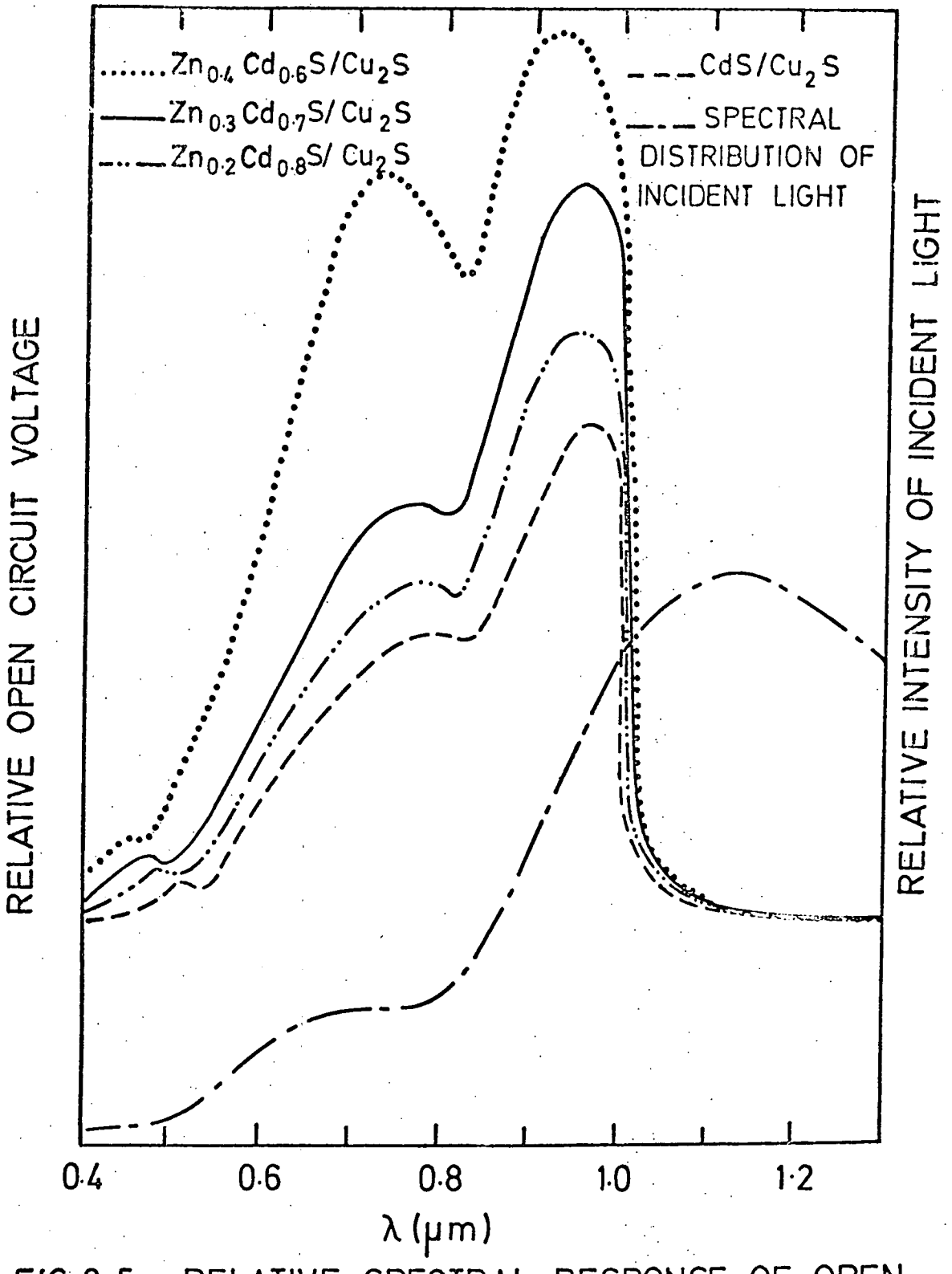


FIG.8·5. RELATIVE SPECTRAL RESPONSE OF OPEN CIRCUIT VOLTAGE AT ROOM TEMPERATURE FOR AS MADE CELLS ON SUBSTRATES OF DIFFERENT COMPOSITIONS.

regardless of the composition of the underlying $Zn_xCd_{1-x}S$. Closer inspection of the two bands reveals that the magnitude of the peak attributed to djurleite increased relative to that associated with chalcocite as the zinc content increased. These observations are in good agreement with the RED studies of the copper sulphide layers on these devices. The other important feature of the spectral response curves in Fig 8.5 is the shift to shorter wavelengths of the peak at 0.52 μm (the CdS bandgap) with increasing zinc content. In Table 8.2 the value of the bandgaps of the various $Zn_xCd_{1-x}S$ solid solutions, calculated from the maximum in the short wavelength spectral response, are compared with the values predicted by the equation proposed by Bennaceur et al[4]. The agreement is excellent.

TABLE 8.2 : The value of the bandgap of the $Zn_xCd_{1-x}S$ solid solutions ($0 \leq x \leq 0.4$).

	CdS	$Zn_{0.2}Cd_{0.8}S$	$Zn_{0.3}Cd_{0.7}S$	$Zn_{0.4}Cd_{0.6}S$
Measured bandgap (eV)	2.42	2.52	2.63	2.72
Theoretical bandgap (eV) Ref (4)	2.42	2.52	2.61	2.72

RED studies of the copper sulphide layer on the sulphur faces of $Zn_xCd_{1-x}S$ single crystals after an air-bake confirmed that the transition towards copper deficient phases also occurred in $Zn_xCd_{1-x}S/Cu_yS$ cells. For instance, when devices on $Zn_{0.2}Cd_{0.8}S$ substrates, which gave rise to a chalcocite dominant RED pattern similar to that shown in Fig 5.11, were baked for 2 minutes in air at 200°C, the resultant RED patterns were similar to that for djurleite (Fig 5.12).

The effect on the spectral response of V_{oc} for a cell formed on a substrate of $Zn_{0.2}Cd_{0.8}S$, after baking in air at 200°C for various lengths of time, is shown in Fig 8.6. Curve A illustrates the response of the as-plated cell with the major band at 0.96 μm. After a 2 minute bake curve B was obtained, showing a large increase in the band at about 0.68 μm and a significant decrease in the longer wavelength band. After a further 2 minute bake, curve C was measured showing that the response at 0.96 μm had almost disappeared and that the peak at shorter wavelength had shifted to about 0.60 μm. The response in the vicinity of the bandgap of the $Zn_{0.2}Cd_{0.8}S$ increased as the treatment was prolonged. Similar effects were observed with cells prepared on substrates of each composition but the replacement of a response similar to that of curve A with one similar to curve C was achieved with significantly shorter baking times with increasing zinc concentrations.

The spectral distribution of V_{oc} and I_{sc} for as-prepared devices on $Zn_xCd_{1-x}S$ substrates was unaffected by additional bandgap bias illumination, which agrees with the observations on as-made CdS/Cu_2S heterojunctions. However, after an air-bake, such bias illumination had a significant effect on the spectral responses. Typical changes in the spectral distribution of V_{oc} and I_{sc} for a 2 minute heat-treated $Zn_{0.3}Cd_{0.7}S$ cell with a different intensity of bias light are shown in Figs 8.7 and 8.8 respectively. As described above after the air-bake, the band at about 0.68 μm increased, while that at 0.96 μm decreased. When the cell was illuminated with secondary bias light, both V_{oc} and I_{sc} showed a quenching band maximum at about 1.35 μm with its onset at about 1.70 μm and an enhancement of the 0.96 μm and the 0.68 μm bands. As the bias light intensity was increased by the same amount curves b, c, and d were obtained for V_{oc} and I_{sc} (Figs 8.7 and 8.8). The important features of these curves are :

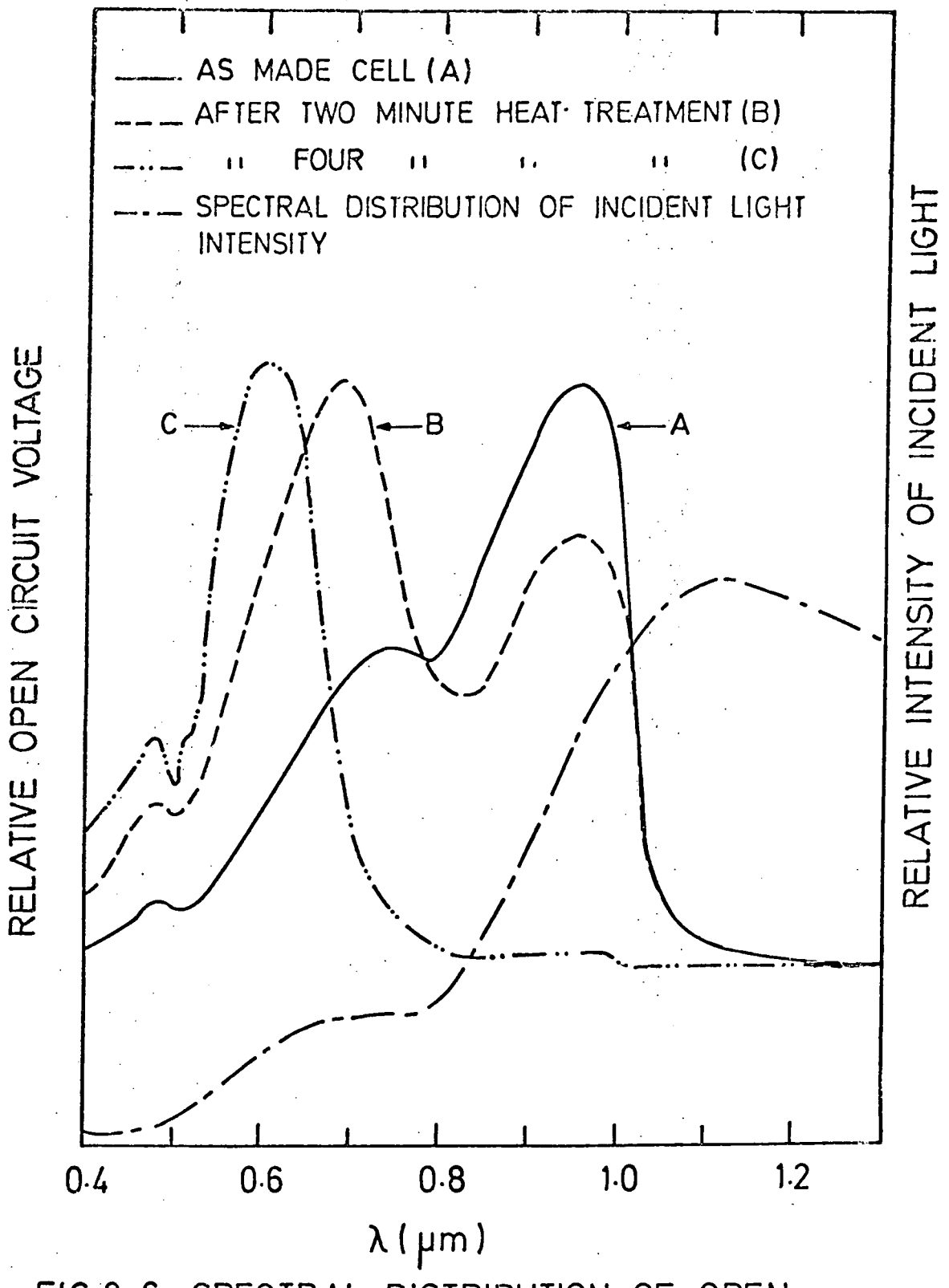


FIG.8·6. SPECTRAL DISTRIBUTION OF OPEN – CIRCUIT VOLTAGE OF $Zn_{0.2}Cd_{0.8}S/Cu_yS$ CELL AS A FUNCTION OF HEAT TREATMENT IN AIR

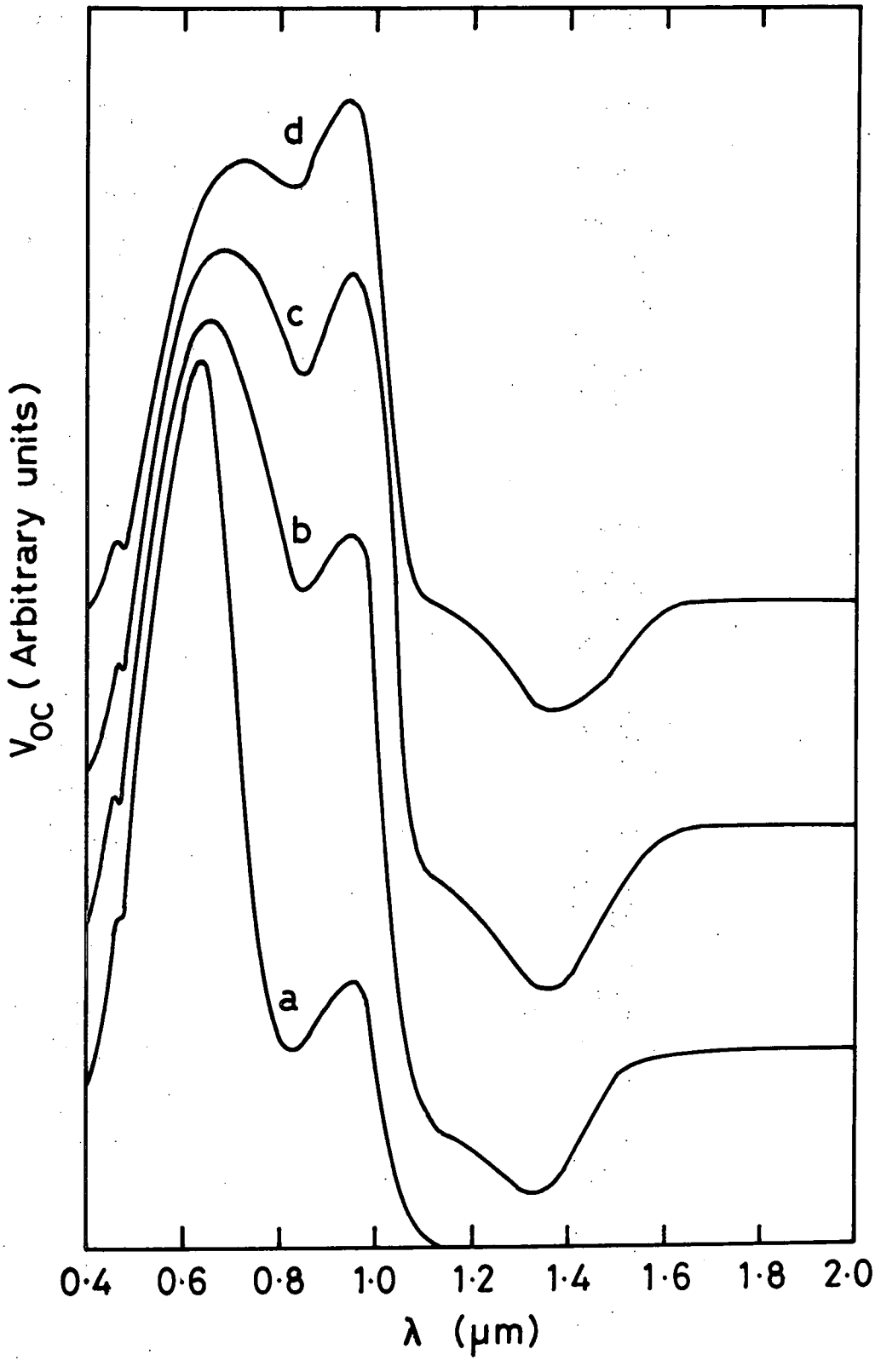


FIG. 8·7 SPECTRAL DISTRIBUTION OF V_{OC} FOR A $Zn_{0.3}Cd_{0.7}S/Cu_yS$ CELL AFTER A 2 MIN. AIR-BAKE (a) WITHOUT BIAS LIGHT, (b, c & d) WITH DIFFERENT VALUES OF BIAS LIGHT INTENSITY.

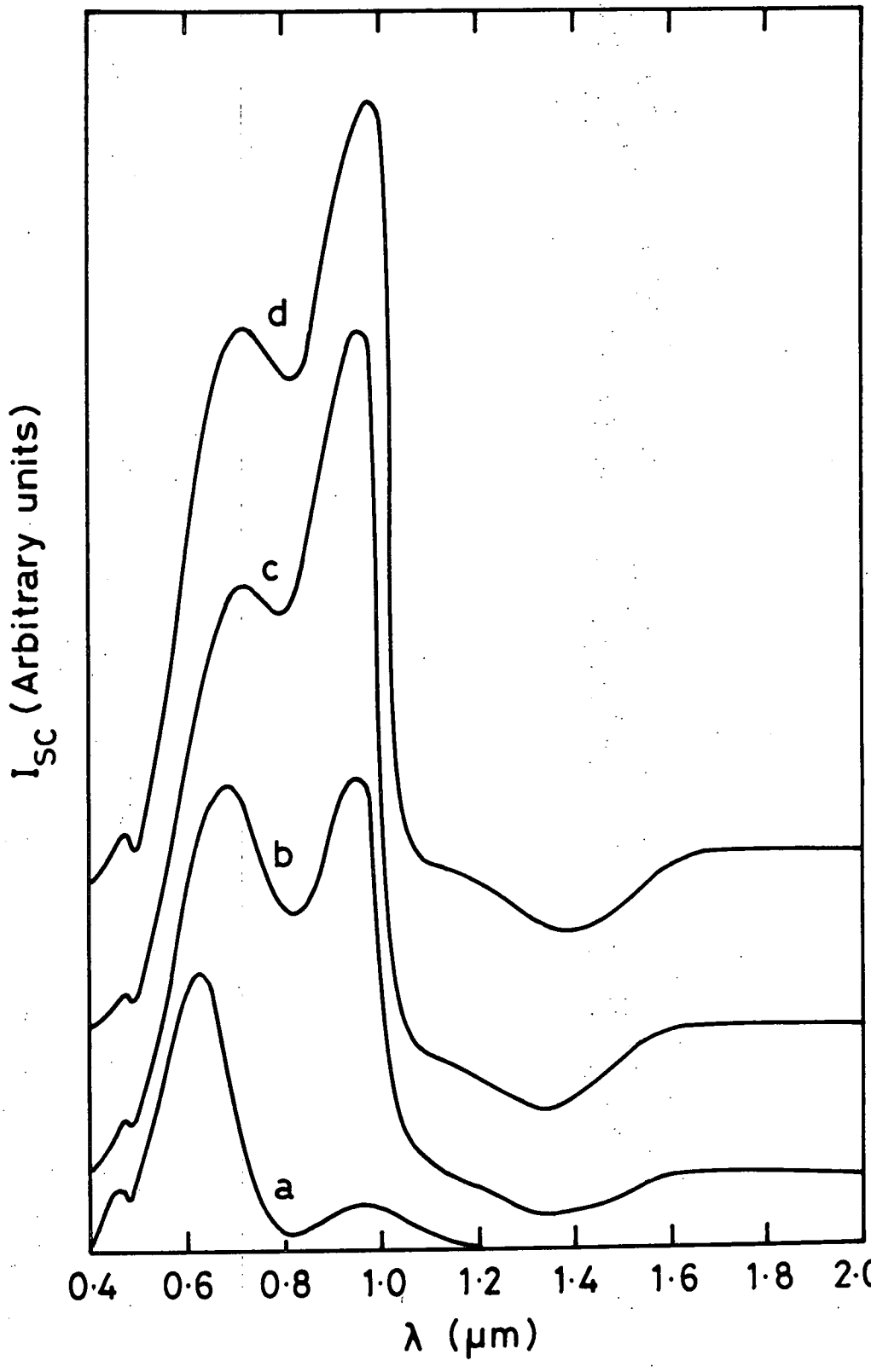


FIG. 8·8 SPECTRAL DISTRIBUTION OF I_{SC} FOR A $Zn_{0·3}Cd_{0·7}S/Cu_yS$ CELL AFTER A 2 MIN. AIR-BAKE (a) WITHOUT BIAS LIGHT (b, c & d) WITH DIFFERENT VALUES OF BIAS LIGHT INTENSITY.

(i) as the intensity of bias light increased the band at 0.96 μm became dominant for both V_{oc} and I_{sc}, but the relative change in the 0.96 and 0.68 μm peaks was larger for I_{sc}, (ii) the band at 0.68 μm shifted to longer wavelengths (at about 0.70 μm) with increasing intensity of the bias light, (iii) while the magnitude of the V_{oc} quenching band decreased, the quenching became more significant in I_{sc} at higher intensities of the bias light, (compare the bands at 1.35 μm in Figs 8.7 and 8.8). As the intensity rose a shoulder appeared on the short wavelength side of the quenching peak (1.24 μm $<\lambda<$ 1.13 μm) in both the V_{oc} and I_{sc} responses.

The spectral responses of heat treated $Zn_xCd_{1-x}S/Cu_yS$ devices of each composition under bias illumination showed similar changes with an increase in two major long wavelength response bands ($\sim$ 0.96 and 0.70 μm), and one definite quenching band at about 1.35 μm, in good agreement with the results on CdS/Cu_xS devices (see Chapter 5, section 5.7.3).

8.5 DARK CURRENT CONDUCTION PROCESS IN $Zn_xCd_{1-x}S/Cu_yS$ HETEROJUNCTIONS

The dark current-voltage characteristics of heterojunctions fabricated on $Zn_xCd_{1-x}S$ mixed crystals have also been investigated. Fig 8.9 shows typical forward and reverse current-voltage characteristics at room temperature for an as-made $Zn_{0.3}Cd_{0.7}S/Cu_yS$ cell. By comparing the curves with those in Fig 7.1, it is obvious that the mechanisms of current flow are similar in nature to those of the corresponding CdS/Cu_2S type A devices. Thus the forward current-voltage characteristics can be divided into three regions. In region I, at low voltages, $\lesssim$0.1 V, the forward current was of similar magnitude to the reverse current. With increasing bias the two characteristics diverged and the forward branch exhibited two regions with different slopes. However, in region II at 0.4 V the rectification ratio was not very high but for current densities greater than 10^{-3} A cm^{-2}, it increased significantly to about 10^{2} (at 0.8 V). When the slopes of two lines were fitted to the usual diode expression for forward current, diode

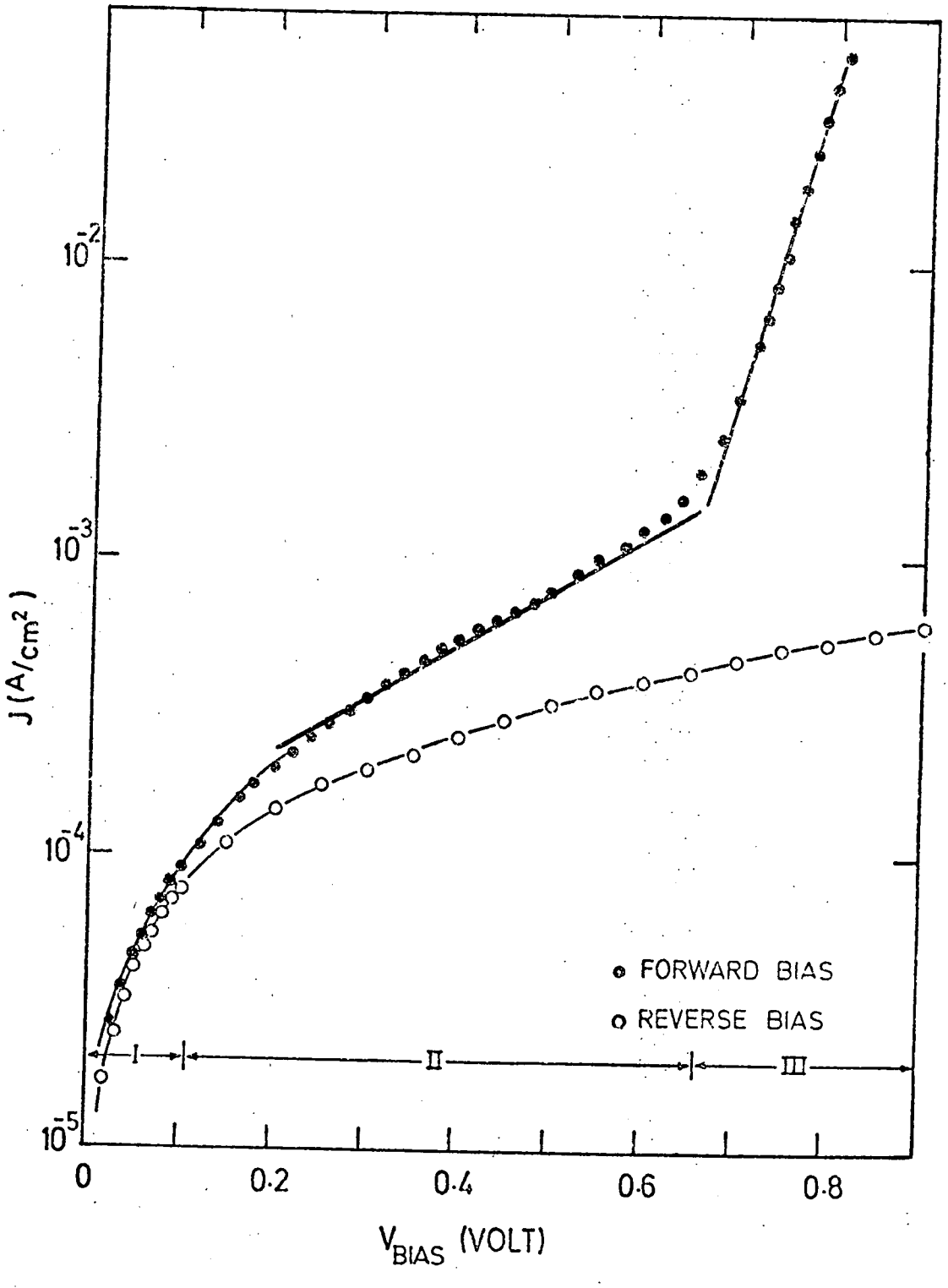


FIG. 8·9. DARK CURRENT–VOLTAGE CHARACTERISTICS FOR AS-MADE $Zn_{0.3}Cd_{0.7}S/Cu_2S$ CELL AT ROOM TEMPERATURE.

factors (A) of 10 and 1.6 were found with corresponding values of the current factor (J_o) of $1.11.10^{-4}$ and $1.44.10^{-10}$ A cm^{-2}, which were obtained by extrapolation of the straight lines in region II and III to zero bias.

The current-voltage characteristics in reverse bias (log-log plot is shown in Fig 8.10) exhibit ohmic behaviour up to 0.5 V, corresponding to a resistivity of 75 k Ω-cm, and thereafter a $J \propto B V^{\gamma}$ relation with a γ value of 1.6 for $0.5 < V_R < 2.5$ V and 2 for $V > 2.5$ V. In general the values of reverse bias at which the mechanisms changed over were found to vary from device to device.

A typical set of forward current-voltage characteristics for an as-prepared $Zn_{0.3}Cd_{0.7}S/Cu_2S$ device measured at various temperatures between 85 K and 295 K is plotted semilogarithmically in Fig 8.11. These curves show that at each temperature the characteristics exhibited approximately the same two distinct regions II and III which began where the carrier density exceeded 10^{-4} and 10^{-3} A cm^{-2}. Once again it is clear that the curves in Fig 8.11 are similar to those in Fig 7.3 for CdS/Cu_2S. The behaviour may be briefly summarized as follows : (i) in region II the current flowing across the junction is a weak function of forward bias and temperature whereas in region III the current is strongly temperature and voltage dependent, (ii) in both regions the slopes of log J_F vs V_F were almost independent of temperature suggesting that current conduction in the $Zn_xCd_{1-x}S/Cu_yS$ junctions is governed by two thermally activated tunnelling recombination mechanisms, with different activation energies.

By using the reverse saturation current (current factor) expression for interface recombination (see Chapter 7, Eq. 7.2), and assuming that the interface recombination velocity (S_I) is 5×10^6 cm/sn[5] and the effective mass (m*) is 0.17 m_o[6], the two activation energies (where the barrier is thin enough for direct tunnelling to the interface states or recombination centres to occur) were calculated to be 0.60 eV and 0.95 eV

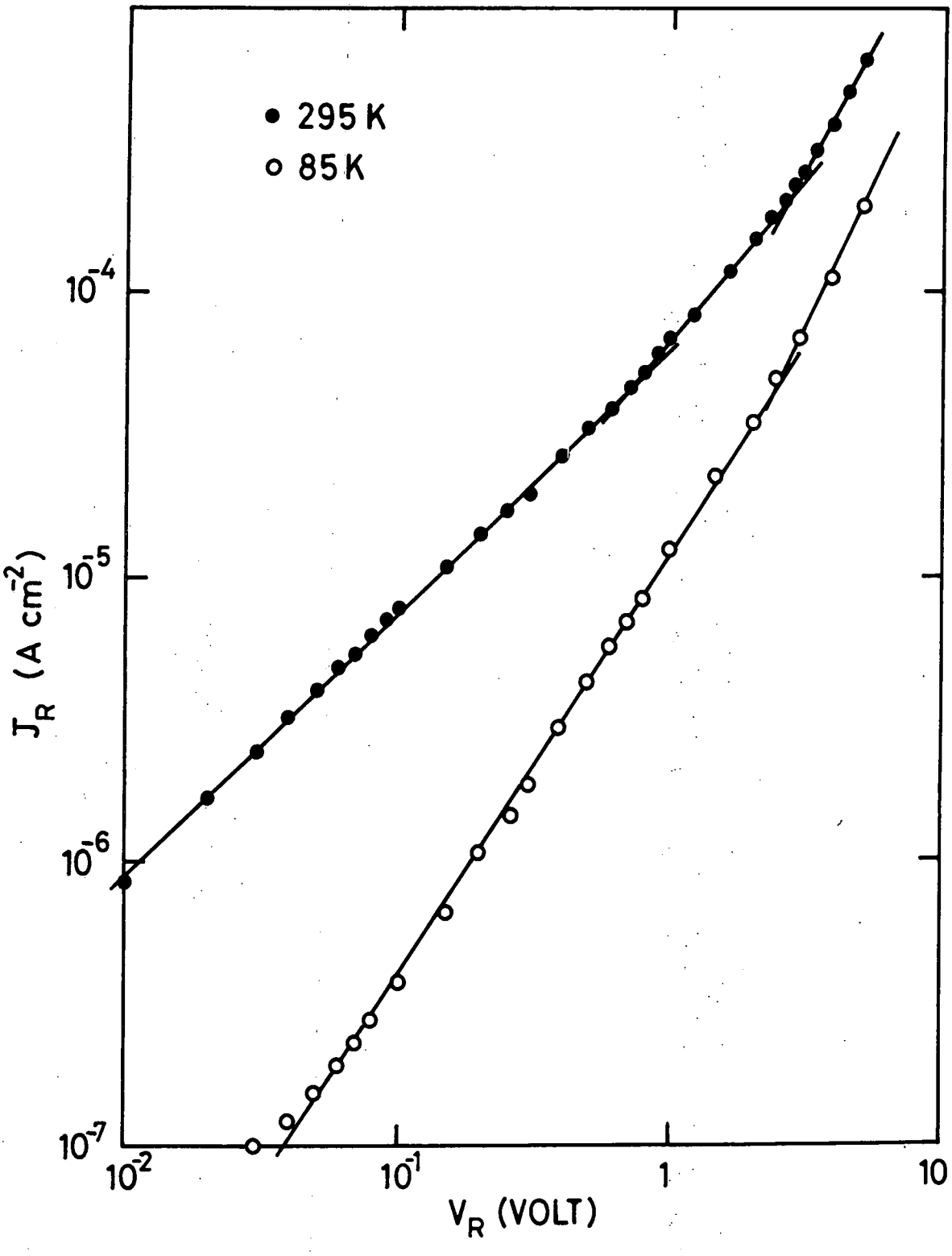


FIG. 8·10 DARK REVERSE CURRENT VOLTAGE CHARACTERISTICS FOR AS-MADE $Zn_{0.3}Cd_{0.7}S$ / Cu_2S CELL AT 85 K AND 295 K

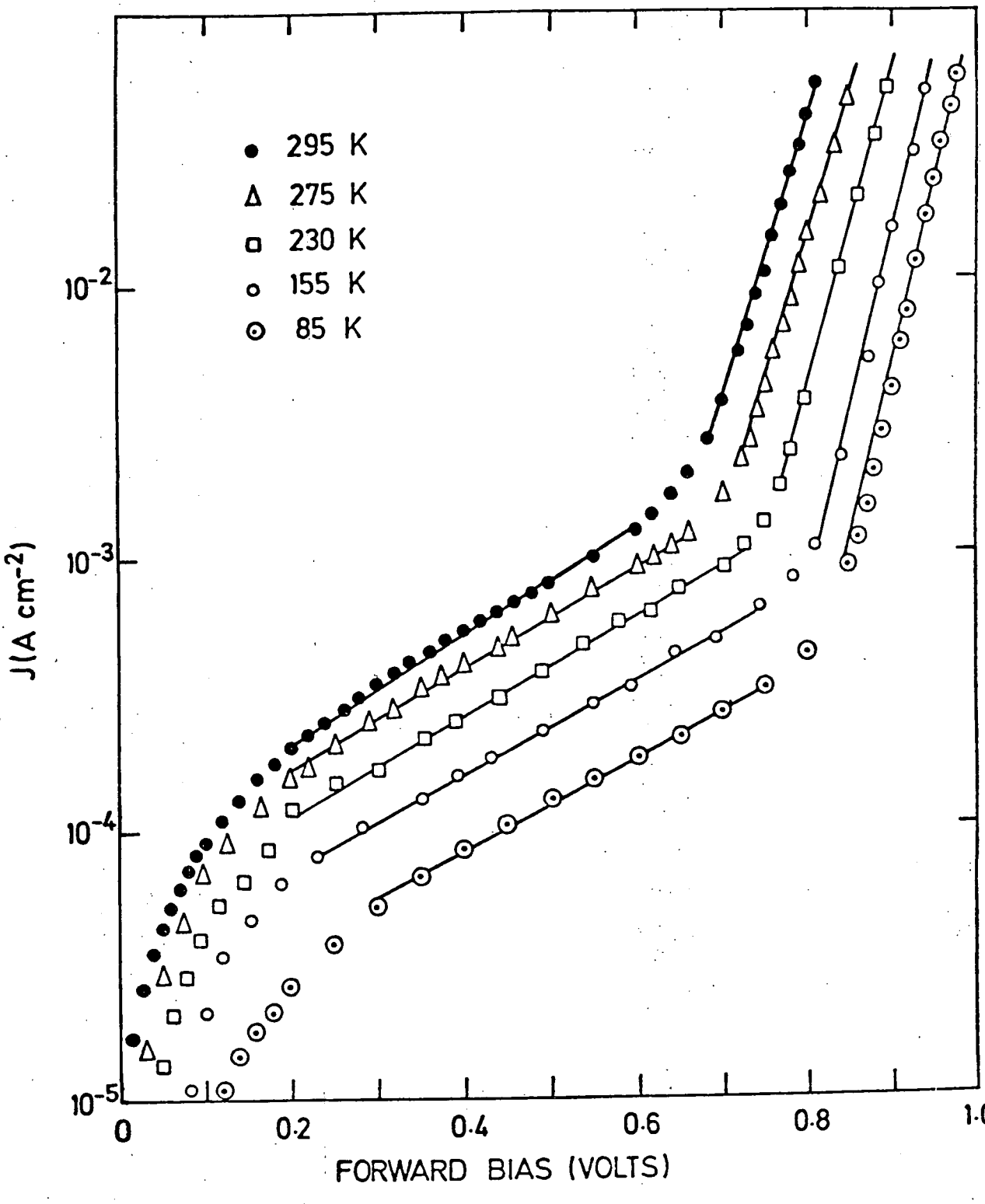


FIG. 8·11 DARK FORWARD CURRENT - VOLTAGE CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR AN AS-MADE $Zn_{0.3}Cd_{0.7}S$ / Cu_2S CELL.

at room temperature from the results in Fig 8.9.

Activation energy analysis on $Zn_xCd_{1-x}S/Cu_yS$ cells as described in section 7.2 for CdS/Cu_2S cell has also been carried out, and activation energies of $\Delta E \tilde{\sim}$ 0.4 and 0.6 eV were calculated from plots of log J_F/T^2 against T^{-1}. As emphasized in Chapter 7, all experiments were conducted below 320 K to prevent copper diffusion during measurements.

The reverse current-voltage characteristics measured at 85 K and 295 K for an as-made $Zn_{0.3}Cd_{0.7}S/Cu_yS$ cell are also shown in Fig 8.10. Unlike the situation in the CdS/Cu_2S cell there was a considerable temperature dependence particularly at low voltages.

After a 2 minute air-bake at 200°C, the dark forward current-voltage characteristics of the $Zn_{0.3}Cd_{0.7}S/Cu_yS$ cell, measured at 85 and 295 K, were as depicted in Fig 8.12. At both temperatures the characteristics also exhibited practically the same distinct slopes. In the first linear region the diode factor (A) improved from 10.00 to 4.63 and the current factor (J_o) from 1.11 10^{-4} to 8.46 10^{-7} A cm^{-2}. By using the same approach as with the as-made sample, the calculated value of the effective barrier for this region was found to have increased from 0.60 to 0.72 eV after the heat treatment. In the second linear region, A improved from 1.6 to 1.5 and J_o from 1.44 10^{-10} to 3.88 10^{-13} A cm^{-2} corresponding to an increase in the effective barrier height from 0.95 to 1.10 eV.

The dark reverse current-voltage characteristics for the $Zn_{0.3}Cd_{0.7}S/Cu_yS$ cell after the 2 minutes air-bake are illustrated in Fig 8.13. These characteristics can also be described by the expression $J \propto V^{\gamma}$, with γ taking the value of 2 when the reverse bias exceeded 0.1 V. The temperature dependence of the reverse current was reduced significantly after the air-bake.

The photothresholds (barrier heights to reverse electron flow) for the excitation of electrons from the copper sulphide to the $Zn_xCd_{1-x}S$ have been determined measuring the photoresponse at photon energies smaller than

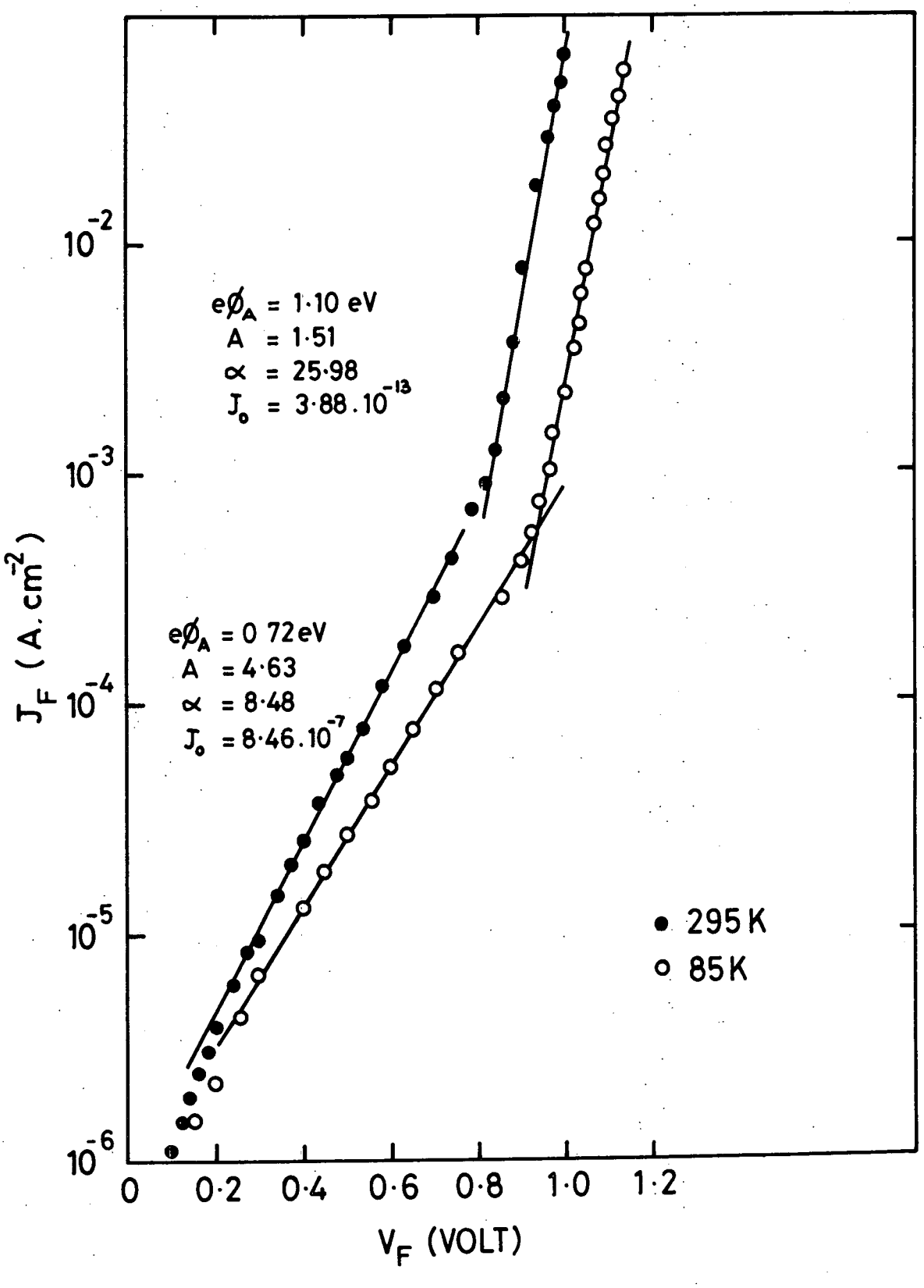


FIG. 8·12 DARK FORWARD CURRENT - VOLTAGE CHARACTERISTICS FOR A 2 MIN. AIR-BAKED $Zn_{0.3}Cd_{0.7}S/Cu_yS$ CELL AT 85K AND 295K

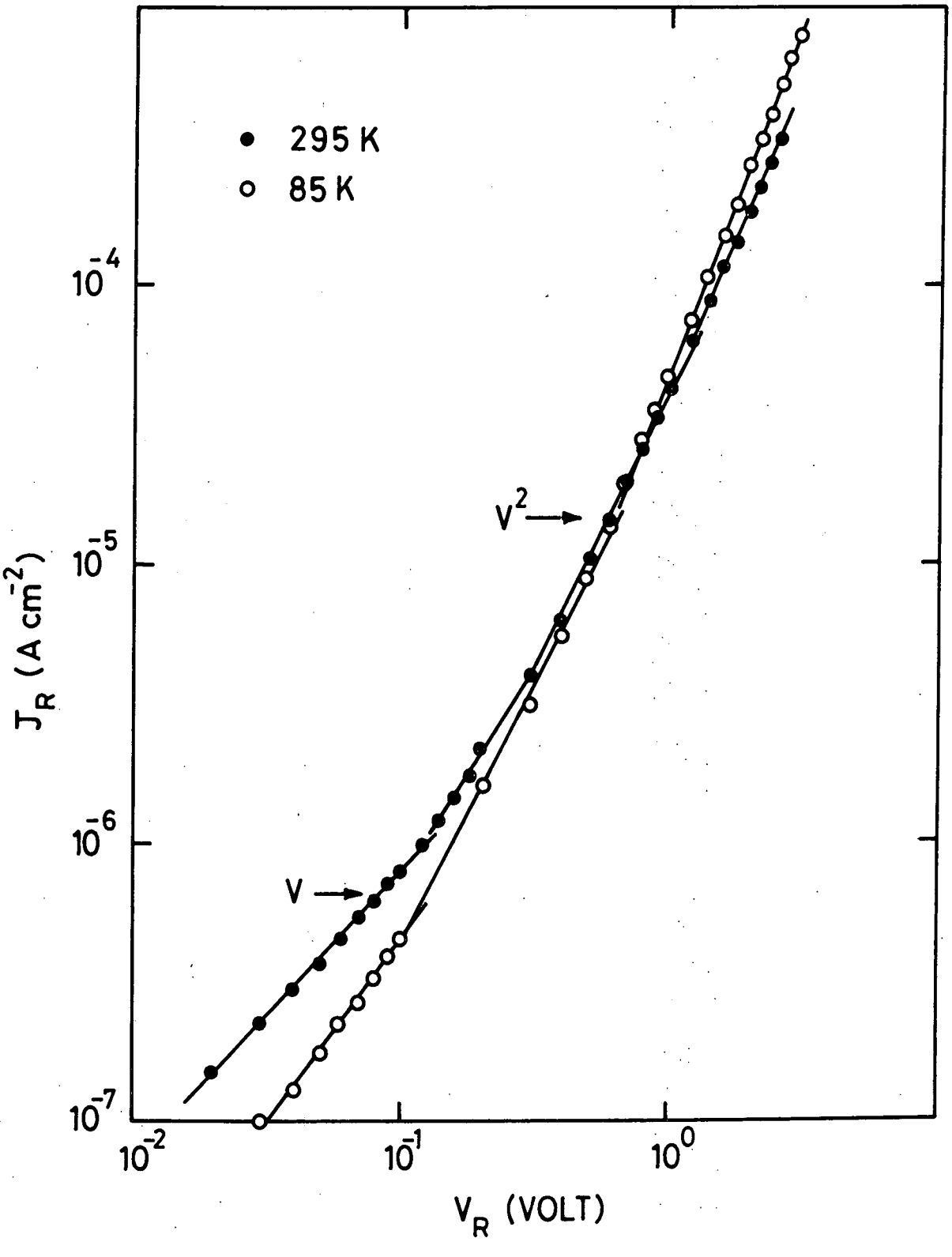


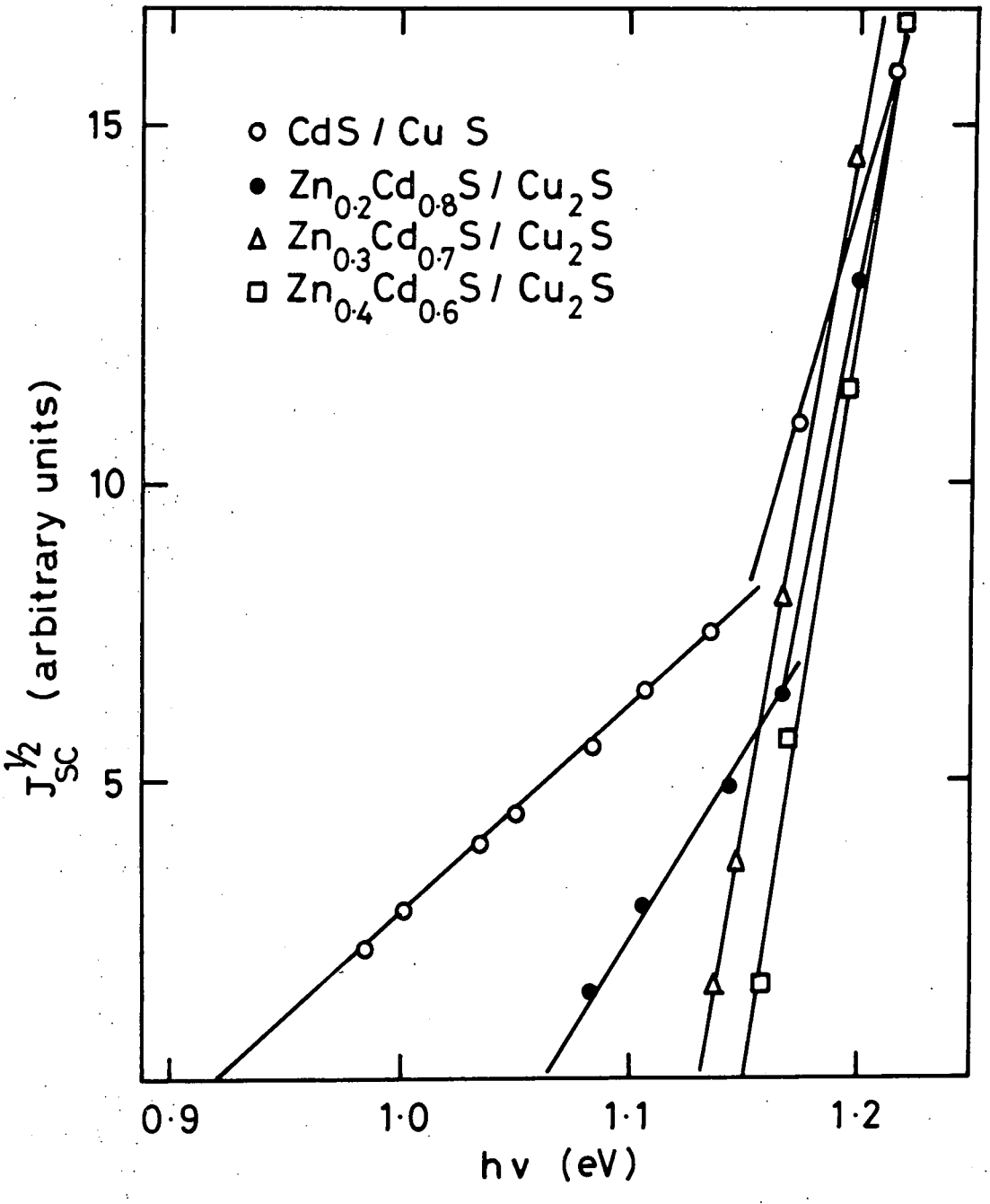
FIG. 8·13 DARK REVERSE CURRENT - VOLTAGE CHARACTERISTICS FOR A 2MIN. AIR-BAKED $Zn_{0.3}Cd_{0.7}S/Cu_yS$ CELL AT 85K AND 295K

the chalcocite bandgap (1.2 eV). The barrier heights were determined by extrapolating the plots of $J_{sc}^{\frac{1}{2}}$ against photon energy shown in Fig 8.14. These measurements demonstrate that the barrier height increased with the zinc content.

For terrestrial application of $Zn_xCd_{1-x}S/Cu_2S$ photovoltaic cells, it is obvious that cells would be used under a various intensity of illumination up to a maximum of 100 mW cm^{-2} (AM1). Thus the dependence of V_{oc} and J_{sc} on the illumination level has also been studied. In broad terms J_{sc} increased linearly with excitation intensity, while there was a logarithmic relation between light intensity and V_{oc}. The experimental points in Fig 8.15 show how V_{oc} and J_{sc} for a $Zn_{0.3}Cd_{0.7}S/Cu_yS$ cell were related when the intensity of illumination was varied from about 100 mW cm^2 down to 1 mW cm^{-2}. Since the plot of log J_{sc} against V_{oc} is linear, Eq. 7.3 is applicable to these heterojunctions. The values of A and J_o calculated from the results plotted in Fig 8.15 are 2.0 and 1.3 10^{-4} A cm^{-2} respectively.

8.6 CAPACITANCE STUDY OF Zn_x-$Cd_{1-x}S/Cu_2S$ HETEROJUNCTIONS

The dark capacitance-voltage measurements on the $Zn_xCd_{1-x}S/Cu_2S$ cells were undertaken to study the space charge distribution in the junction. The technique used has already been described in Chapter 4, section 4.7. A C-V characteristic, in the form $1/C^2$ against V, is shown in Fig 8.16 for an as-made $Zn_{0.3}Cd_{0.7}S/Cu_2S$ cell. In general, for heterojunctions based on $Zn_xCd_{1-x}S$, $1/C^2$-V plots exhibited two slopes corresponding to regions with different carrier concentrations. By using the conventional formula, the calculated net donor densities for $Zn_{0.3}Cd_{0.7}S$ were about 1.79 10^{16} cm^{-3} near the junction and about 3.46 10^{16} cm^{-3} further from the junction. This may be taken as an indication of zinc compensation near the junction. The depletion region calculated from dark zero bias capacitance was about 0.55 μm for this particular device. Voltage intercepts, when $1/C^2$ was extrapolated to zero, were extremely high.



	$CdS-Cu_2S$	$Zn_{0.2}Cd_{0.8}S-Cu_2S$	$Zn_{0.3}Cd_{0.7}S-Cu_2S$	$Zn_{0.4}Cd_{0.6}S-Cu_2S$
Photo-electric threshold (eV)	0.92	1.07	1.13	1.15

TABLE II

FIG. 8·14 SQUARE ROOT OF THE PHOTORESPONSE PER INCIDENT PHOTON AGAINST PHOTON ENERGY FOR AS MADE CELLS ON SUBSTRATES OF DIFFERENT COMPOSITIONS.

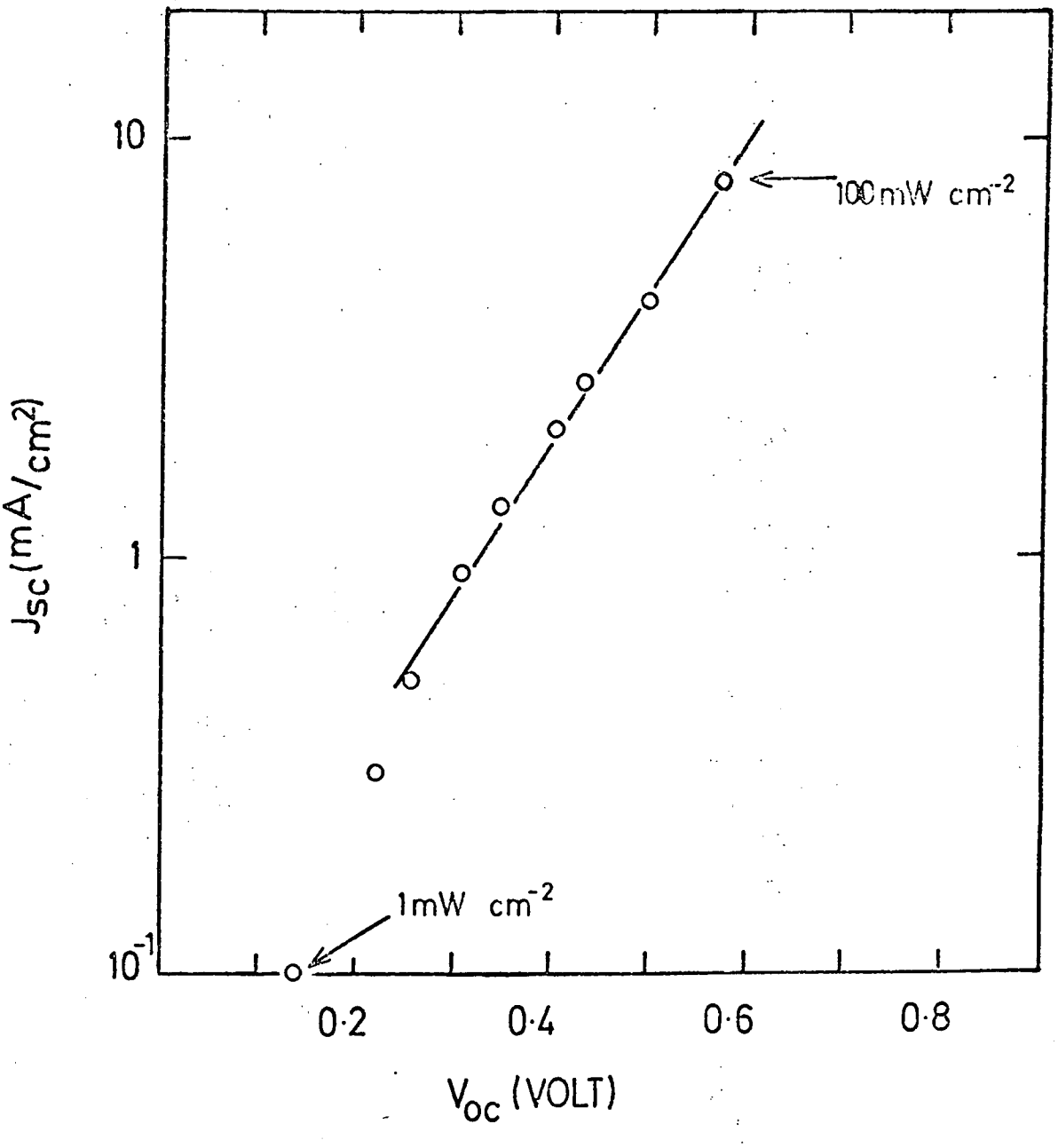


FIG.8·15. THE DEPENDENCE OF SHORT CIRCUIT CURRENT ON OPEN CIRCUIT VOLTAGE AS A FUNCTION OF INTENSITY OF ILLUMINATION FOR $Zn_{0.3}Cd_{0.7}S/Cu_2S$ AS-MADE CELL

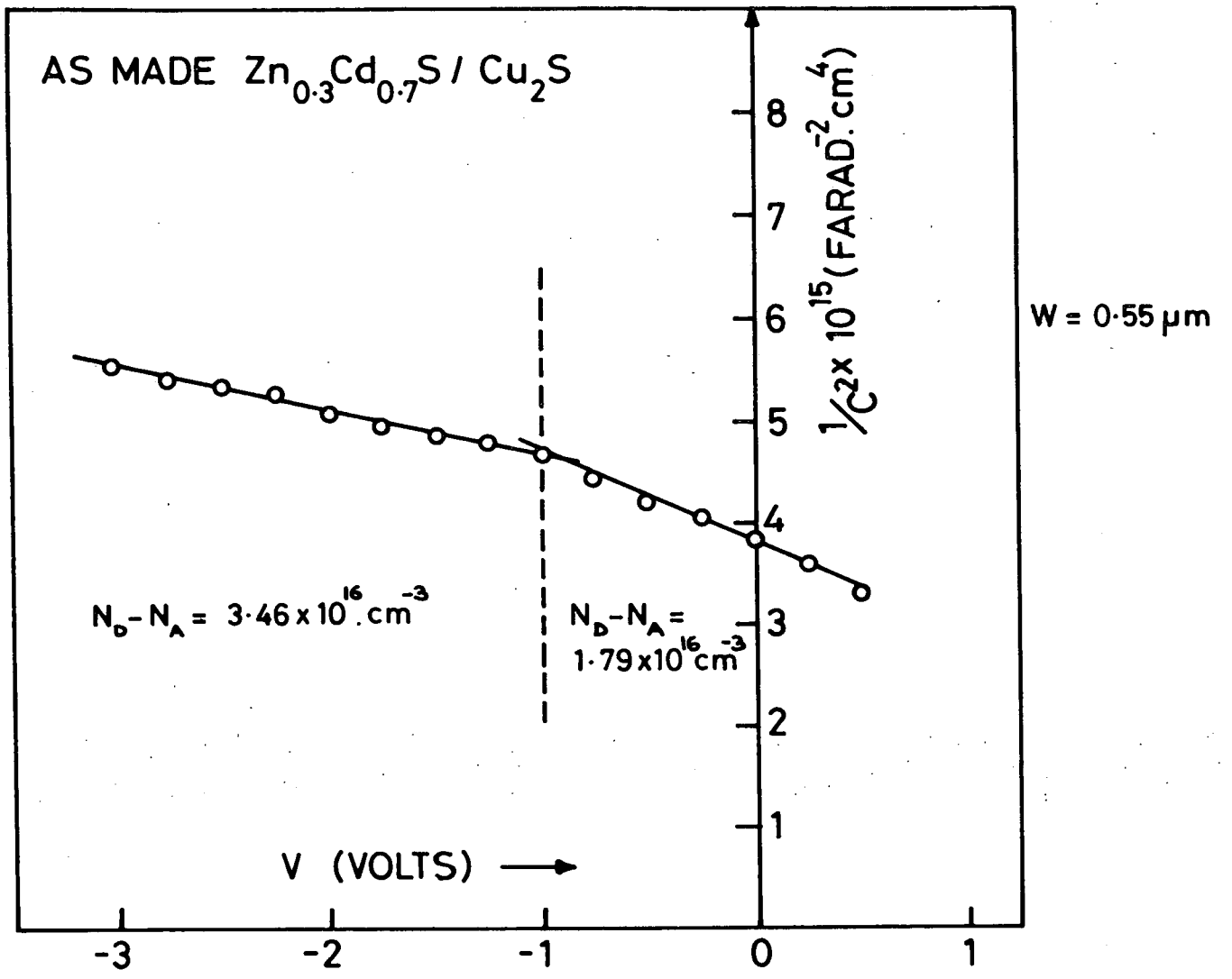


FIG. 8·16. C^{-2} VERSUS V_R PLOT FOR AN AS-MADE $Zn_{0.3}Cd_{0.7}S$ / Cu_2S CELL

8.7 DISCUSSION AND CONCLUSION

The work described in this chapter has shown that satisfactory, homogeneous single crystals of $Zn_xCd_{1-x}S$ can be successfully grown with Zn compositions up to 30 molar percent from the vapour phase. X-ray measurements of the lattice parameters show that both a_o and c_o decrease sublinearly with zinc composition (see Fig 8.1) in a manner similar to that reported earlier for evaporated thin film materials[7,8]. Thus the aim of matching the lattice of copper sulphide (Cu_2S has an a_o value of 11.848 or $a_o/3 = 3.949$ Å) should be satisfied with a mixed crystal of approximate composition $Zn_{0.4}Cd_{0.6}S$. This is in good agreement with Böer's theoretical prediction of $x = 0.46$[9].

In a crystal with such a composition, where the contribution to the density of interface states from lattice mismatch is minimised, it is expected that the major source of interface states will be a function of the surface topography of the substrate. This suggestion is supported by the EBIC observations of the devices fabricated on type A and B $Zn_xCd_{1-x}S$ surfaces with different numbers of ledges and kink sites on the etch hillocks. As with the CdS cells (see Chapter 6, section 6.3), the regions of the junction at kink sites and ledges correspond to areas where the current collection is smaller than elsewhere, so that such regions have smaller interface collection factors. Extending this interpretation to the overall properties of the devices, the dramatic influence of the surface topography on device characteristics is explained in the same way as was done for CdS devices in Chapter 5.

The increase in V_{oc} and the simultaneous decrease in J_{sc} with increasing zinc content (see Fig 8.3) for our $Zn_xCd_{1-x}S/Cu_2S$ cells prepared on single crystal substrates agrees with the results previously reported for thin films devices[3,9,10,11,12]. The increase in V_{oc} with rising zinc content is similar to the increase in the values of photothreshold measured over the same composition range (compare Table 8.1 and 8.3). These values of threshold

imply that the photoexcited electrons cross the junction via interface states without reaching the conduction band of Cu_2S. It is widely accepted that the electron affinity of CdS exceeds that of Cu_2S by 0.2 eV[11] so that an observed photothreshold of 0.92 eV indicates that tunnelling starts to occur via a level 0.08 eV below the bottom of the conduction band of CdS, since the bandgap of Cu_2S is 1.2 eV. Although there is no published data on the variation in electron affinity of $Zn_xCd_{1-x}S$ alloys, it is generally assumed that this parameter decreases as the zinc content increases. As a result the difference in electron affinities of Cu_2S and $Zn_xCd_{1-x}S$ ($\Delta\chi$) should be reduced. Indeed, the threshold measurements confirm that this happens. However, after the addition of a certain amount of zinc to the CdS lattice, $\Delta\chi$ is expected to become negative causing a potential spike to be formed in the conduction band. Because of the decrease in the lattice mismatch and the associated reduction in the interface state density, the probability of tunnelling via these states is decreased. Thus the better match in the electron affinity and the lattice parameter (a_o) work together to improve the effective barrier height at the junction with increasing zinc content. In fact by substituting the value of reverse saturation current for interface recombination $J_o = qN_c S_I \exp(-q\phi_B/kT)$ into equation (7.3) a direct relation between V_{oc} and $q\phi_B$ can be written as

$$V_{oc} \approx A\phi_B + \frac{AkT}{q} \ln\left[\frac{J_{sc}}{q N_c S_I}\right]$$

Using the values given in Table 8.1 and taking $N_c = 2.3\ 10^{18}\ cm^{-3}$, $S_I = 5 \times 10^6$ cm/sn, the calculated values $q\phi_B$ became about 0.95 eV for CdS/Cu_2S and 1.21 eV for $Zn_{0.4}Cd_{0.6}S/Cu_2S$ devices. These values are not far from what was observed experimentally (see Fig 8.14 and Table 8.3). Thus the increase in V_{oc} can be attributed almost entirely to the barrier improvement. A reduction in the interface recombination velocity and increase

in effective barrier height with rising zinc content should enhance the interface collection factor, which in turn should give rise to large values of J_{sc} in $Zn_xCd_{1-x}S$ cells, but this was not observed experimentally. In fact there was a monotonic reduction in J_{sc} with zinc content, which has also been reported by many workers on thin film devices[3,9,10,11,12]. Other factors apparently are also operative. One such possibility might be associated with the different ion-exchange kinetics involved in forming copper sulphide on $Zn_xCd_{1-x}S$ instead of CdS. Burton[11] demonstrated that the zinc composition varies both vertically and laterally at the interface of a plated $Zn_xCd_{1-x}S/Cu_yS$ heterojunction which he explained in terms of smaller values of solubility and diffusion coefficient of Zn^{++} relative to those of Cd^{++} in Cu_yS and the different ratios of the exchange reactions in different crystallographic directions. Our electron diffraction studies showed that it became more difficult to produce a uniform phase of chalcocite as the zinc content of substrates was increased. Some djurleite was always detected in the layers plated on $Zn_xCd_{1-x}S$. At higher zinc compositions (i.e. $Zn_{0.4}Cd_{0.6}S$) djurleite became the dominant phase. These observations were confirmed by the spectral response measurements of cells with high zinc composition plated under the same conditions. Two pronounced long wavelength bands in V_{oc} and J_{sc}, corresponding to the bandgap of chalcocite and djurleite, were apparent for each composition. However, the peak associated with djurleite (0.70 μm) increased in magnitude relative to that attributed to chalcocite (0.96 μm) as the zinc content was increased. In addition to the difficulty of converting $Zn_xCd_{1-x}S$ to the desired phase of copper sulphide, SEM examination of the cross-section of these heterojunctions also revealed that the thickness of the converted layer decreased considerably with rising zinc concentration. A similar observation was recently reported by the Delaware group[13].

A further complication with the copper sulphide layer formed on $Zn_xCd_{1-x}S$ substrates is associated with the difference in the solubility and the diffusion coefficients of Zn^{++} and Cd^{++} in these layers. It is now known that with CdS substrates, about 0.27 mol% cadmium exists in copper sulphide layers formed by aqueous ion exchange[14]. Burton[15] has demonstrated that concentrations of about 3×10^{19} cm^{-3} of cadmium and 7×10^{19} cm^{-3} of zinc are retained in a copper sulphide formed on thin film substrates. Okomoto and Kawai[16] and Bougnot[17] suggested that the donor doping effects of the divalent ion could be beneficial through the compensation of the copper vacancies in copper sulphide. However Burton[15] has concluded that the quantities of zinc and cadmium retained in the copper sulphide are not significant to influence the absorption coefficient, diffusion length and resistivity of the copper sulphide. Thus the reduction in J_{sc} probably does not result from variations in the concentration of zinc and cadmium in the copper sulphide. The results reported here indicate that the preferential formation of copper deficient phases of copper sulphide, coupled with a decrease in the thickness of the converted layer as the zinc content of substrate was increased, would certainly lead to a reduction in J_{sc}.

The potential spike in the conduction band is not expected to appear until $X > 0.2$[11], if the ion exchange process proceeds with the correct stoichiometry. However Burton[15] has demonstrated that the cuprous ion solution in which the $Zn_xCd_{1-x}S$ is converted into copper sulphide is deficient in zinc compared to the Zn/Cd ratio of the bulk of the substrate. Since only very small amounts of cadmium and zinc are retained in copper sulphide, the extra zinc (relative to the cadmium) is likely to accumulate in (CdZn)S beneath the junction. Thus the actual zinc in the substrate close to the junction probably differs from the bulk value. This excess zinc could lead to an anomalously high resistivity regime (zinc rich) close to the interface, which in turn could give rise to a potential spike at the interface even if the zinc concentration in the bulk was not sufficiently high to produce one. That

this might happen is supported by capacitance-voltage measurements on $Zn_xCd_{1-x}S/Cu_2S$ heterojunctions which suggest a junction profile with lower carrier concentrations near the junction (see Fig 8.16). If these ideas are correct, the potential energy diagram would be as shown in Fig 8.17[18], and as the spike developed in the conduction band J_{sc} would decrease appreciably.

The other possible effects of a zinc rich region could be to reduce the electron mobility (μ_e) and the electric field at the interface. There are unfortunately very few reports of the electron mobility in $Zn_xCd_{1-x}S$ alloys. However, Sakurai et al[19] and Feigelson et al[20] have found that the electron mobilities in (Zn Cd)S materials are independent of composition. Thus changes in the electric field might be more important. Since the interface collection factor $\beta = \mu F/(S_I + \mu_e F)$, the improvement in its value by a reduction in S_I as the Zn content increases, is probably offset by a decrease in the electric field (F).

The photocapacitance measurements on as-made $Zn_xCd_{1-x}S/Cu_2S$ heterojunctions have shown that the capacitance was practically unchanged by the illumination which suggests that there was no copper at all in the interfacial region of $Zn_xCd_{1-x}S$. Thus any change in the electric field at the interface is not attributable to copper in as-made cells. The spectral response of V_{oc} and J_{sc} of as-prepared $Zn_xCd_{1-x}S/Cu_yS$ cells, with or without secondary bandgap illumination, shows no difference other than a constant shift which offers further confirmation of an illumination independent interface collection factor, which is affected strongly by the zinc rich region at the interface.

Using a different approach Böer[9] has suggested that a potential spike exists even when x = o, and that this spike is transparent to electrons. As x increases the spike decreases in amplitude but its width increases. The increased width makes tunnelling more difficult and thus reduces J_{sc}.

A post barrier air-bake at 200°C did not have a beneficial effect on any of the cells prepared on mixed crystal substrates. The observed changes

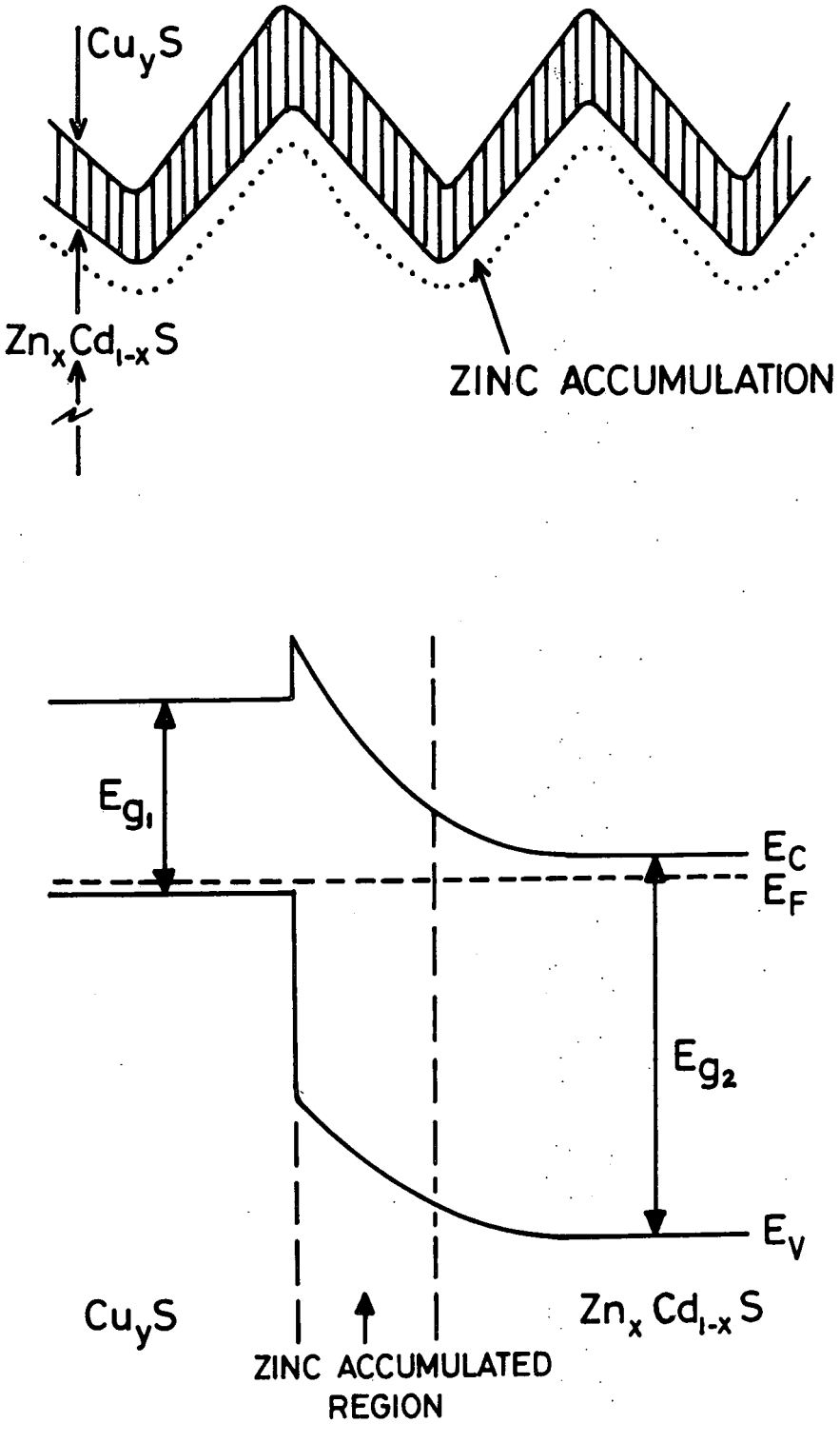


FIG. 8·17. SCHEMATIC DIAGRAM OF $Zn_xCd_{1-x}S/Cu_yS$ JUNCTION CROSS-SECTION AND BAND DIAGRAM FOR THESE HETROJUNCTIONS.

in the spectral responses provided an additional support for the existence of increasing copper deficient phases in the Cu_xS as the Zn content was increased (see Fig 8.6). It was found for example that the duration of the bake required to convert a response similar to curve A (Fig 8.6) to one similar to curve B became shorter as x increased.

A comment is perhaps also required to explain why baking a cell on $Zn_{0.2}Cd_{0.8}S$ for 4 mins (Fig 8.6) shifted the peak of the spectral response from 0.70 μm (bandgap of djurleite) to 0.62 μm. It could be that the peak at 0.62 μm is a super-position of the effects of optical absorption in the copper sulphide layer and of deep levels in the depletion region of $Zn_{0.2}Cd_{0.8}S$ associated with the in-diffusion of copper during the bake. It is indeed shown in Chapter 5 that the response of the hexagonal phase of copper sulphide is centred at about 0.63 μm (see Fig 5.22). The shift in Fig 8.6 might also be explained by the Moss-Burstein effect[23] which supposes that increasing degeneracy in the copper sulphide layer is accompanied by an increase in the effective bandgap. A similar explanation for the shift of the spectral response of CdS/Cu_yS cells to shorter wavelengths following heat treatment has been put forward by Kantariya et al[24] and recently by Rothwarf and Windawi[25].

The increase in the response at the bandgap of $Zn_{0.2}Cd_{0.8}S$ as baking proceeded, suggested that the copper sulphide layer was becoming more transparent as the copper deficient phases developed, which is consistent with the evidence that Cu_2S has the highest optical absorption of all the copper sulphide phases[22].

The effects observed with bias illumination, e.g. the enhancement of the peaks in the vicinity of 0.7 and 0.96 μm and the appearance of the infrared quenching band at about 1.35 μm in the photovoltaic spectral response of heat treated cells, can be explained in the same way as similar effects in CdS/Cu_yS cells were explained in Chapter 7, section 7.6. Thus a post barrier

air-bake leads to migration of copper into $Zn_xCd_{1-x}S$ compensating the substrate near the junction. However, because of the zinc rich region at the junction, even a small amount of copper diffusion will result in a considerable compensation in $Zn_xCd_{1-x}S$ interfacial region. Consequently after the heat treatment the electric field at the junction which controls the interface collection factor, would be dependent on the density of diffused copper. From the preliminary photocapacitance measurements during infra-red quenching the copper levels were found to be located at about 0.30 eV and 1.2 eV above the valence band, which are the same as the copper levels found in the heat treated CdS/Cu_yS cells. Because of the coincidence between the transition energies to the copper levels at $\sim$ 1.2 eV above the valence band and the chalcocite bandgap, the quenching peak at this energy was not observed in the photovoltaic response of heat treated cells (see Figs 8.6, and 8.7).

Analysis of the dark current-voltage characteristics of $Zn_xCd_{1-x}S/Cu_2S$ cells indicated that the forward current conduction process in these heterojunctions is also governed by thermally activated tunnelling recombination processes. In general, the forward J-V characteristics of as-prepared cells can be regarded as being composed of two thermally activated tunnelling recombination processes operating at different current levels, which can be compared to a certain extent with the processes already discussed for the CdS/Cu_2S heterojunction in Chapter 7, section 7.6. The main difference lies with the temperature dependences in the low voltage region (< 0.2 V). With CdS/Cu_2S cells the forward J_F-V_F characteristics measured at different temperatures converged towards one another at low voltages (see Fig 7.3) whereas with $Zn_xCd_{1-x}S/Cu_2S$ devices the characteristics still exhibited a temperature dependence (see Fig 8.11). This suggests that tunnelling recombination via interface states with energies close to the bottom of the

conduction band is reduced due to the improved lattice match between $Zn_xCd_{1-x}S$ and Cu_2S. The same explanation can also be used to account for the difference in the reverse bias characteristics of CdS and $Zn_xCd_{1-x}S$ based cells as a function of temperature (compare Figs 7.2 and 8.10). Apart from these two discrepancies, the forward and reverse current conduction processes in as-made $Zn_xCd_{1-x}S/Cu_2S$ heterojunctions can be explained in the same way as for CdS/Cu_2S devices in Chapter 7. A post barrier air-bake at 200°C has also improved the dark diode characteristics of $Zn_xCd_{1-x}S/Cu_yS$ heterojunctions. This can be explained in the same way as the CdS/Cu_2S cells in a following manner ; in-diffused copper compensates the $Zn_xCd_{1-x}S$ at the interfacial layer after the heat treatment and in addition the air-bake enhances the absorption of oxygen at the interface where it forms electron traps. These two effects improve the barrier height in the dark (Compare Figs 8.9 and 8.12). However the forward and reverse conduction mechanisms put forward to explain the processes in as-made samples are still valid after the air-bake (see Figs 8.12 and 8.13).

The work described in this chapter has demonstrated that the behaviour of cells prepared on single crystals of $Zn_xCd_{1-x}S$ with zinc composition in the range $0 \leq X \leq 0.4$ is comparable in many respects with that of devices made on thin film substrates. By working with single crystals, the complications associated with grain boundaries and the surface texture of thin films, etc. are avoided. Well defined junctions were produced on oriented $Zn_xCd_{1-x}S$ substrates. This allowed us to investigate the several possible mechanisms that could account for differences between the cells fabricated on $Zn_xCd_{1-x}S$ and CdS single crystal substrates. The surface preparation and the resultant surface topography is also of paramount importance to the characteristics of $Zn_xCd_{1-x}S/Cu_2S$ cells. As the zinc content of the substrate is increased, it becomes more difficult to produce the desired phase and thickness of copper sulphide.

The increase in V_{oc} with increasing zinc composition is attributed to an increase in the barrier height due to improved lattice and electron affinity match between $Zn_xCd_{1-x}S$ and Cu_2S. Although the decrease in J_{sc} could not be attributed to one specific mechanism, it is suggested that copper deficient phases of thinner copper sulphide layers and the excess zinc in the substrate at the interface are the major causes of this reduction. Finally, it has been shown that the forward current conduction mechanisms in $Zn_xCd_{1-x}S/Cu_2S$ cells are also dominated by thermally activated tunnelling recombination processes, and the reverse current processes obey an ohmic law at low voltages, then follow the Zener current law. In summary, the model proposed for CdS/Cu_2S cells in Chapter 7 (see Figs 7.23),in conjunction with the band diagram given for $Zn_xCd_{1-x}S/Cu_yS$ heterojunction (see Fig 8.17), can explain most of the observations on these devices.

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CHAPTER 9

SUMMARY AND CONCLUSIONS

The main objective of the work described in this thesis was to investigate the major processes involved in the fabrication of CdS/Cu_2S and $Zn_xCd_{1-x}S/Cu_2S$ photovoltaic cells and to determine what effects variations in these processes had on the electronic and optoelectronic characteristics of the finished devices. Thus the influence of each of the fabrication stages on the ultimate behaviour of the cells has been established, and the conditions for the preparation of devices with optimum performance have been determined.

Examination of substrate surfaces prior to junction formation showed that the process of surface polishing to remove the saw marks produces a thin polycrystalline sphalerite layer of either CdS or $Zn_xCd_{1-x}S$. Obviously the subsequent etching of CdS (or $Zn_xCd_{1-x}S$) was really a two-stage process involving (1) the removal of the polycrystalline layer and (2) the etching of the underlying hexagonal single crystal. Apart from affecting the etching behaviour, the polycrystalline layer had an adverse influence in that any device made on a polished surface had poor characteristics. With both CdS and $Zn_xCd_{1-x}S$ crystals, the sequence of cutting and polishing was found to have a considerable effect on the ultimate nature of the etched surfaces. The surface of an etched die which had been polished as a slice, consisted of an array of smoothly facetted hillocks (type A surface), whereas the surface of an etched die which had been polished after being cut from a slice was characterised by a large number of ledges, terraces and kink sites (type B surface). To account for the differences it is suggested that the polishing of a relatively large area, as in the preparation of type A surfaces, leads to a polycrystalline cubic

layer of uniform thickness, whereas polishing an individual die leads to greater non uniformity, not least because of the increased difficulty of keeping it flat to maintain a uniform distribution of force during the polishing process. As the chemical dissolution proceeds through a non-uniform polycrystalline layer the etchant may reach the hexagonal single crystal bulk in some regions before others. This, in conjunction with the expected difference in etch rates of the polycrystalline layer and the single crystal material, are thought to be the main factors determining the ultimate topography of etched surfaces.

By preparing a large number of devices on type A and type B surfaces it has been shown that there is a direct correlation between the overall surface topography and the resultant device characteristics. Devices made on type A surfaces consistently exhibited very good diode characteristics and excellent photovoltaic performance in their as-prepared condition, while in contrast, devices fabricated on type B surfaces were always poor in this state. A similar relationship between surface topography and device characteristics has been reported for thin film CdS/Cu_2S cells (i.e. see Ref (15) and (24) in Chapter 5). However, the complexities of grain boundaries and different grain orientations in thin film cells do not allow a correlation to be made between device characteristics and specific surface features, in the way that is possible with devices made on single crystal substrates. Examination in the SEM allowed the influence of specific surface features on the device characteristics to be revealed on a microscopic scale. Examination of surfaces in the EBIC mode showed that the existence of kink sites and ledges gave rise to dark EBIC contrast regions in which the EBIC current was smaller than that associated with regions of light contrast. Indeed EBIC studies of CdS/Cu_2S and Zn_xCd_{1-x}/Cu_2S cells in parallel with their examination under optical radiation have demonstrated that there is a direct correlation between

optical and electron beam excitation. Thus it was possible to investigate the photovoltaic behaviour of cells at a microscopic level by operating the SEM in the stationary spot mode and measuring current-voltage characteristics. In this way it was established more specifically that there is a direct correlation between the loss of local photovoltaic sensitivity and the ledges and kink sites on etched hillocks. Consequently, it is concluded that the growth of copper sulphide on etched CdS and $Zn_xCd_{1-x}S$ is complicated by the presence of kink sites and ledges on etch hillocks, leading to the production of a higher local density of interface states. This conclusion explains the pronounced differences observed between the characteristics of type A and type B devices in their as-made state.

Regardless of the topography of etched surfaces, devices formed on very low resistivity material ($\rho \lesssim 0.05\ \Omega$ -cm) did not display any rectification or photovoltaic effect in the as-plated condition. This is attributed to the extremely small depletion width in CdS of this resistivity which gives rise to tunnelling or impact ionization effects in the high field region of the junction.

An investigation concerned with the chemiplating process in which the surface layer of the CdS is converted into copper sulphide has demonstrated that after making three modifications to the customary chemiplating technique the phases of copper sulphide could be produced in a much more controllable manner. The standard procedure adopted for the production of chalcocite (which is the desired phase for solar cell applications) employed a plating bath at a temperature of $95^{o}C$ with a pH of 2.5 and a dipping time of 10s. To achieve further control and maintain comparability with thin film cells, plating was carried out on etched $(000\bar{1})$ faces of CdS and $Zn_xCd_{1-x}S$ single crystals. One result of the RED studies was that it was found that the proportion of djurleite in the copper sulphide became greater on the mixed crystal substrates. Reflection electron diffraction

studies and spectral response measurements of devices carrying different phases of copper sulphide in their as-prepared condition allowed the photovoltaic response at 0.96 μm to be assigned to chalcocite while the response at 0.70 μm was attributable to djurleite. The phase of the copper sulphide layer grown was not particularly dependent on the surface topography but was strongly dependent on the temperature and pH value of the plating bath.

The conversion rate of CdS to copper sulphide was a strong function of crystallographic direction and surface condition (etched or polished). Conversion was faster on etched $(000\bar{1})$ surfaces, and thickness measurements on these surfaces indicated that the rate of growth of the copper sulphide layer followed a parabolic law after 20s dipping time. However, the same law does not hold for dipping times shorter than 20s, and it is assumed that initially the growth rate is controlled by the interface when the thickness of the converted layer increases linearly. The growth rate also decreases with increase in Zn content in the substrates.

Baking CdS/Cu_2S and $Zn_xCd_{1-x}S/Cu_2S$ cells in air at 200°C revealed that this treatment improves the efficiency of type B cells after an optimum baking time of 2 minutes. In contrast the same treatment reduces the efficiency of type A devices. Thus a post barrier air-bake is only beneficial for cells which have poor operational parameters in their as-prepared condition (either because they have type B surfaces or low substrate resistivity). However, for cells with good characteristics (because of their type A surfaces and suitable substrate resistivity) there is no advantage to be gained from the air-bake. In fact undesirable effects of air-baking degrade the performance of these cells. Thus when CdS/Cu_2S and $Zn_xCd_{1-x}S/Cu_2S$ single crystal photovoltaic cells are prepared under controlled and optimized conditions which involve the surface preparation, the bulk resistivity of substrates and the correct stoichiometry and thickness of the copper sulphide

layers, then such cells will have optimum performance in the as-made condition and their stability is good.

By determining the lattice parameters of $Zn_xCd_{1-x}S$ single crystals it has been demonstrated that both a_o and c_o decrease sublinearly with zinc composition, and a perfect lattice match is expected when copper sulphide is grown on $Zn_{0.4}Cd_{0.6}S$. With this composition the open circuit voltage, V_{oc} increased to 0.72 V, but unfortunately there was a considerable decrease in the short circuit current, J_{sc}. It was suggested that the increase in V_{oc} can be directly attributed to an increase in the barrier height due to the improved lattice match between $Zn_xCd_{1-x}S$ and copper sulphide. The explanations proposed for the reduction in J_{sc} are : (i) the increase in the proportion of copper deficient phases in the copper sulphide layer with increasing zinc content, (ii) a decrease in the thickness of the converted layers on the substrates containing more zinc (iii) an accumulation of zinc at the interface on the ZnCdS side which results in a spike in the conduction band continuum.

The measurements of minority carrier diffusion lengths on both sides of the junctions revealed that the values in copper sulphide are independent of the type of surface on which it is grown and the phase of copper sulphide. However, the surface preparation prior to the junction formation did affect the diffusion lengths measured in CdS. The air-bake had no effect on the diffusion length in copper sulphide, but reduced the value in the cadmium sulphide. It seems unlikely that the change in J_{sc} after an air-bake can be attributed to any change in diffusion lengths because 90% of the carrier generation occurs in the copper sulphide in which L_n is not affected by the post barrier treatment.

The dark current conduction process in the CdS/Cu_2S and $Zn_xCd_{1-x}S/Cu_2S$ heterojunctions has also been investigated. In both types of device the dominant current conduction process is one of thermally activated

tunnelling recombination via interface states. With as-made type A devices, two different mechanisms were operative with different activation energies whereas with type B devices only one mechanism with a small activation energy was observed. After an air-bake all devices displayed similar characteristics with two thermally activated tunnelling processes operative. A model was postulated to explain the experimental results which consist of a distributed network of diodes each with different characteristics. Modified band models have been proposed for two situations where (i) tunnelling occurs at energies very close to the bottom of the conduction band of the CdS or (ii) at energies close to the theoretical barrier height. With these models the experimental observations can be explained qualitatively while the quantitative values obtained fit extremely well.

APPENDIX

Au-CdS SCHOTTKY DIODES

In addition to the work reported in this thesis a few attempts were made to investigate Au-CdS Schottky barriers prepared by vacuum evaporation of gold on to chemically etched $(000\bar{1})$ surfaces of CdS single crystals. The main objective of this study was to eliminate the complexities associated with CdS/Cu_2S heterojunctions and to analyze the capacitance-voltage and current-voltage characteristics as well as the spectral response of the photoemission current in a simple metal-semiconductor structure.

The capacitance-voltage measurement, at 100 kHz on all the Schottky diodes examined, yielded straight lines when C^{-2} was plotted against the reverse bias, V_R, (see Fig A.1). This indicates that abrupt junctions were always obtained after depositing gold on etched $(000\bar{1})$ surfaces. Indeed, even for very small bias voltages the C^{-2} versus V plot maintained its linearity confirming the constant density of donors (N_D) in the voltage range used (up to -3.0 V). Calculated values of N_D (from the slopes of the C^{-2} -V plots), for diodes on substrates obtained from different boules varied between $6.87\ 10^{15}$ and $8.84\ 10^{16}$ cm^{-3}. Assuming an electron mobility of 300 $cm^2\ V^{-1}\ s^{-1}$ for CdS, the calculated values of electrical conductivity, σ, ($\sigma = q\ \mu_n N_D$) ranged from 0.33 $\Omega^{-1}\ cm^{-1}$ to 4.24 $\Omega^{-1}\ cm^{-1}$. These calculated results are in good agreement with the measured conductivity values of between 0.40 and 4.50 $\Omega^{-1}\ cm^{-1}$. The width of the depletion regions at zero bias, W_d, were calculated from the relation $W_d = \varepsilon\varepsilon_o A/C_o$ where the dielectric constant ε_{CdS} is 8.64 [1] and C_o/A was the dark capacitance value at zero bias. The values obtained varied between 0.08 μm and 0.15 μm. The diffusion voltages V_d were inferred from the intercepts in the C^{-2} vs V.plots on the voltage axes. The values obtained ranged between 0.46 V and 1.27 V.

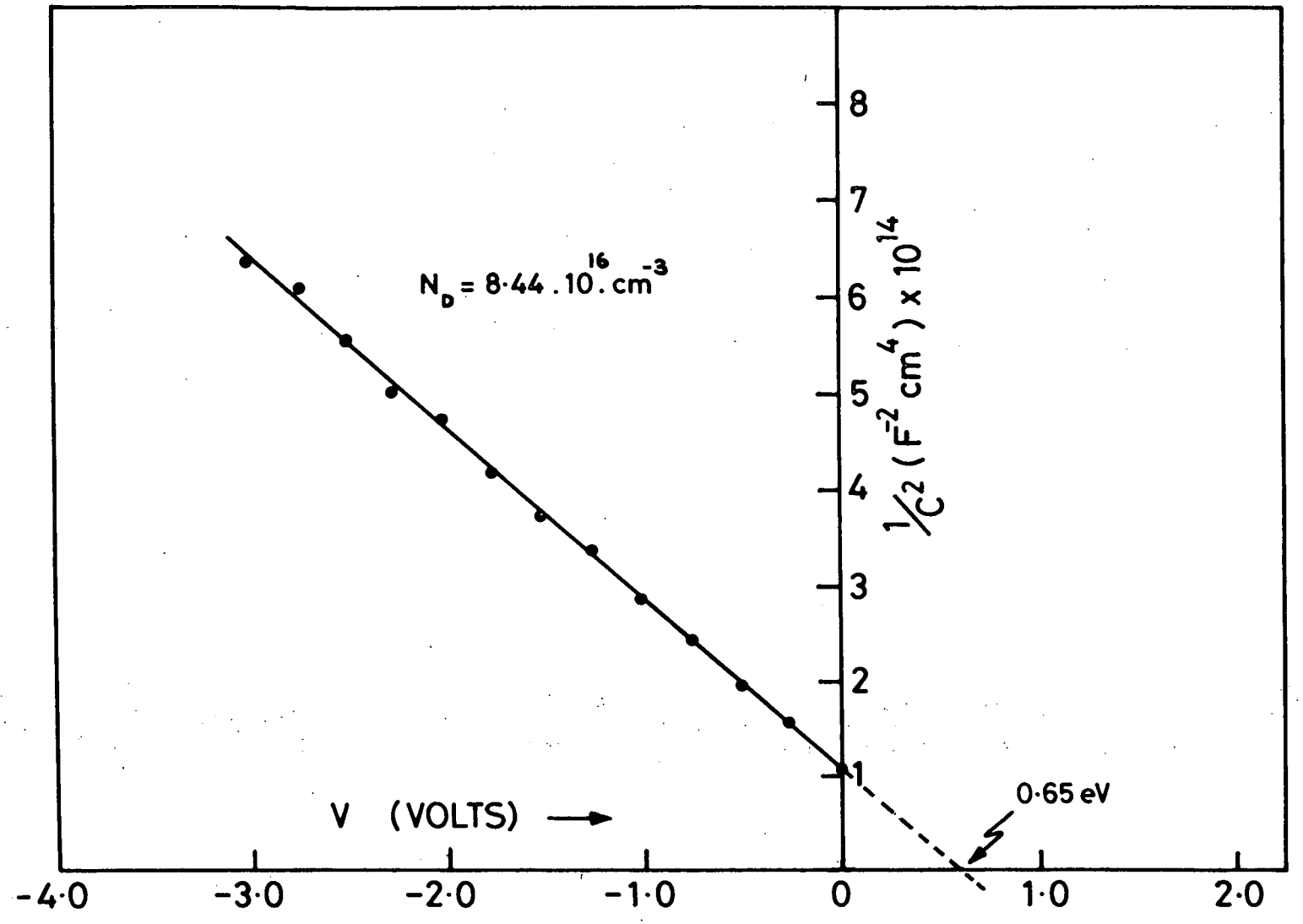

FIG. A·1. C^{-2} VERSUS VOLTAGE FOR AN Au - CdS SCHOTTKY BARRIER DIODE (MEASURED AT 100 kHz).

Despite this variation in the value of V_d, the photothresholds measured from the intercepts of the $\sqrt{R}$ vs $h\nu$ plot on the energy axes (where R represents the photoemission current per incident photon) were very consistent ranging between 0.73 and 0.75 eV. Fig A.2 shows a typical $\sqrt{R}$ versus $h\nu$ plot for the device used to obtain the C^{-2} vs V plot in Fig A.1. For this particular diode the depth of the Fermi level below the conduction band, ξ, was calculated to be 0.085 eV. Thus the barrier height predicted by the equation

$$\phi_B = V + \xi + \frac{kT}{q} \qquad (A.1)$$

(the image force lowering is neglected), was 0.76 eV. In fact for this and a number of other devices fair agreement was obtained between the measured photothreshold value and the barrier height calculated from V_d, however with several others widely different values were obtained although the devices were prepared under identical conditions.

The spectral response of the short-circuit photocurrent in an Au-CdS Schottky barrier diode is illustrated in Fig A3. Although the responses at 85 and 296 K were quite similar, there was a significant shift to shorter wavelengths at 85 K. The short wavelength response suggests that the absorption edge of the CdS increased from 2.42 to 2.54 eV as the temperature was reduced from 296 K to 85 K. These values are in excellent agreement with the conventional expression for the temperature dependence of the bandgap of CdS (see Chapter 2.2). This shift also correlated reasonably well with the increase in the barrier height from 0.74 to 0.86 eV for the same temperature decrease. The parallel shift in the bandgap and the barrier height is taken as an indication that the Fermi level at the Au-CdS interface is pinned[2].

The current-voltage characteristics of Au-CdS diodes have shown a wide variation. The curves in Fig A.4 are log J-V plots for a good Schottky diode at room temperature. The forward current which is typical for most good

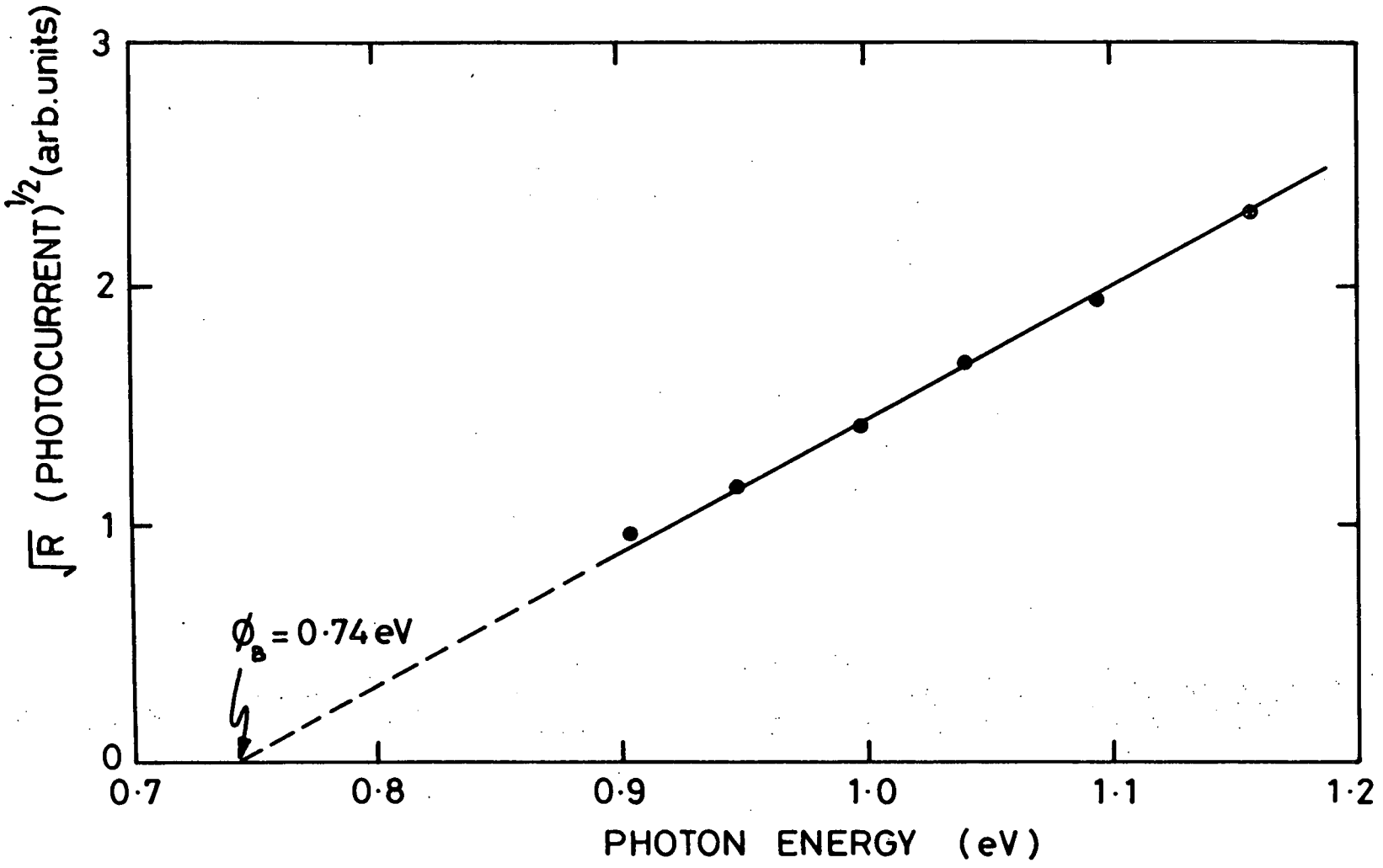

FIG. A 2 SQUARE ROOT OF THE CORRECTED PHOTOCURRENT VERSUS PHOTON ENERGY FOR AN Au - CdS SCHOTTKY BARRIER DIODE .

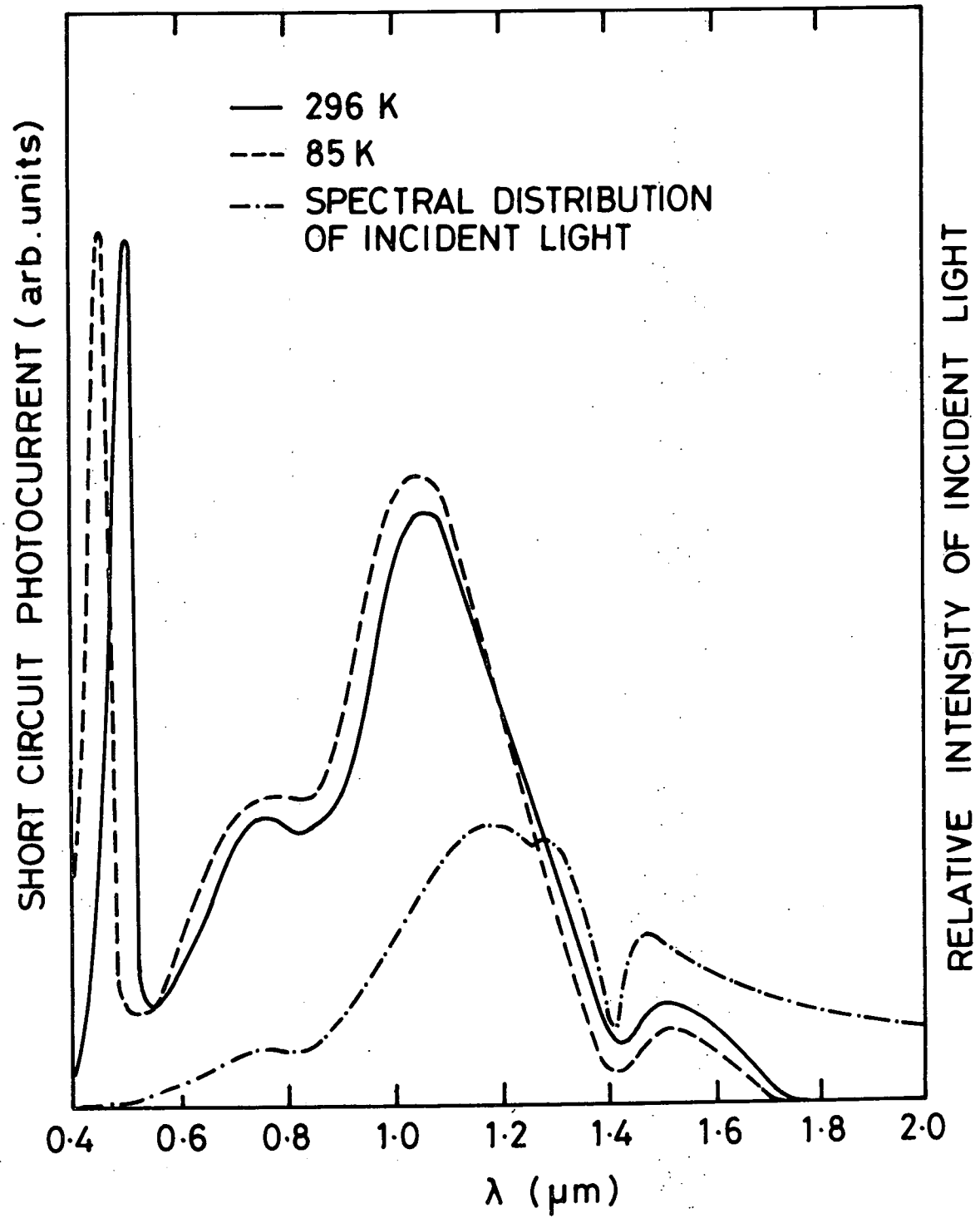

FIG. A·3 THE SPECTRAL RESPONSE OF THE SHORT CIRCUIT PHOTOCURRENT IN AN Au-CdS SCHOTTKY BARRIER MEASURED AT 85K AND 296K.

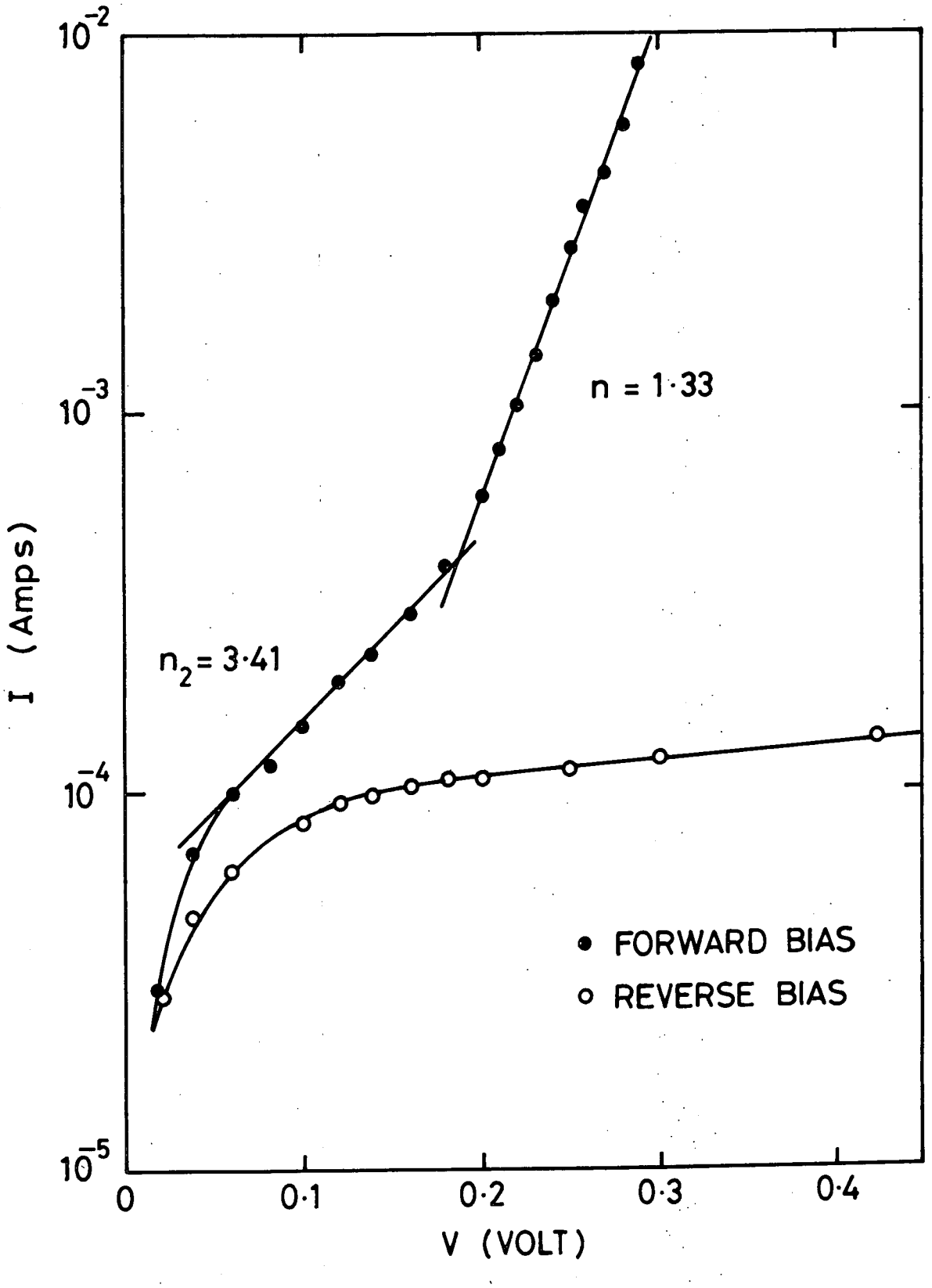

FIG. A·4 DARK CURRENT - VOLTAGE CHARACTERISTICS FOR A GOOD Au - CdS SCHOTTKY BARRIER DIODE MEASURED AT 296 K.

Schottkys can be divided into three regions, (i) a very low voltage region (V_F 0.04 V) in which the reverse and forward current are practically the same and obey Ohm's law, (ii) a region of high saturation current, and ideality factor (J_o = 4.84 10^{-6} mA/cm^2 and n = 3.41), (iii) a region where these parameters have more reasonable value, i.e. n = 1.33 and J_o = 1.68 10^{-7} mA/cm^2.

If the experimental values of J_o in region III is taken with the theoretical value of the Richardson constant (A^* = 25.2 A/cm^2 K^2) [3] the barrier height is found to be 0.62 V (see Eq.3.21). However, the same equation cannot be applied in region II because the ideality factor is so high (n = 3.41).

Nevertheless, the temperature dependence of the forward current showed that the slopes of the log J_F - V_F plots are almost independent of temperature (see Fig A.5). Following the discussion on current mechanisms in CdS/Cu_2S and (CdZn)S/Cu_2S heterojunctions, it is suggested that the forward current in these Schottky diodes are governed by thermally activated tunnelling recombination processes. Thus Eq. 7.2 can also be used here to determine barrier heights. The barrier height for region II is calculated to be 0.50 eV. The reverse current in these diodes did not reach a saturation and increased gradually with applied bias.

The current-voltage characteristics of a poor Schottky diode are plotted semilogarithmically in Fig A.6. A forward current is dominated by region II in this type of diode. Once again, because the ideality factor is considerably larger than unity (n = 2.79) a straightforward thermionic emission theory cannot be applied. However, the temperature independent slopes of log J_F versus V_F plot indicate that thermally activated tunnelling recombination is also operative in the poor devices, the barrier height determined from the appropriate equation (see Chapter 7, Eq. 7.2) was about 0.48 eV.

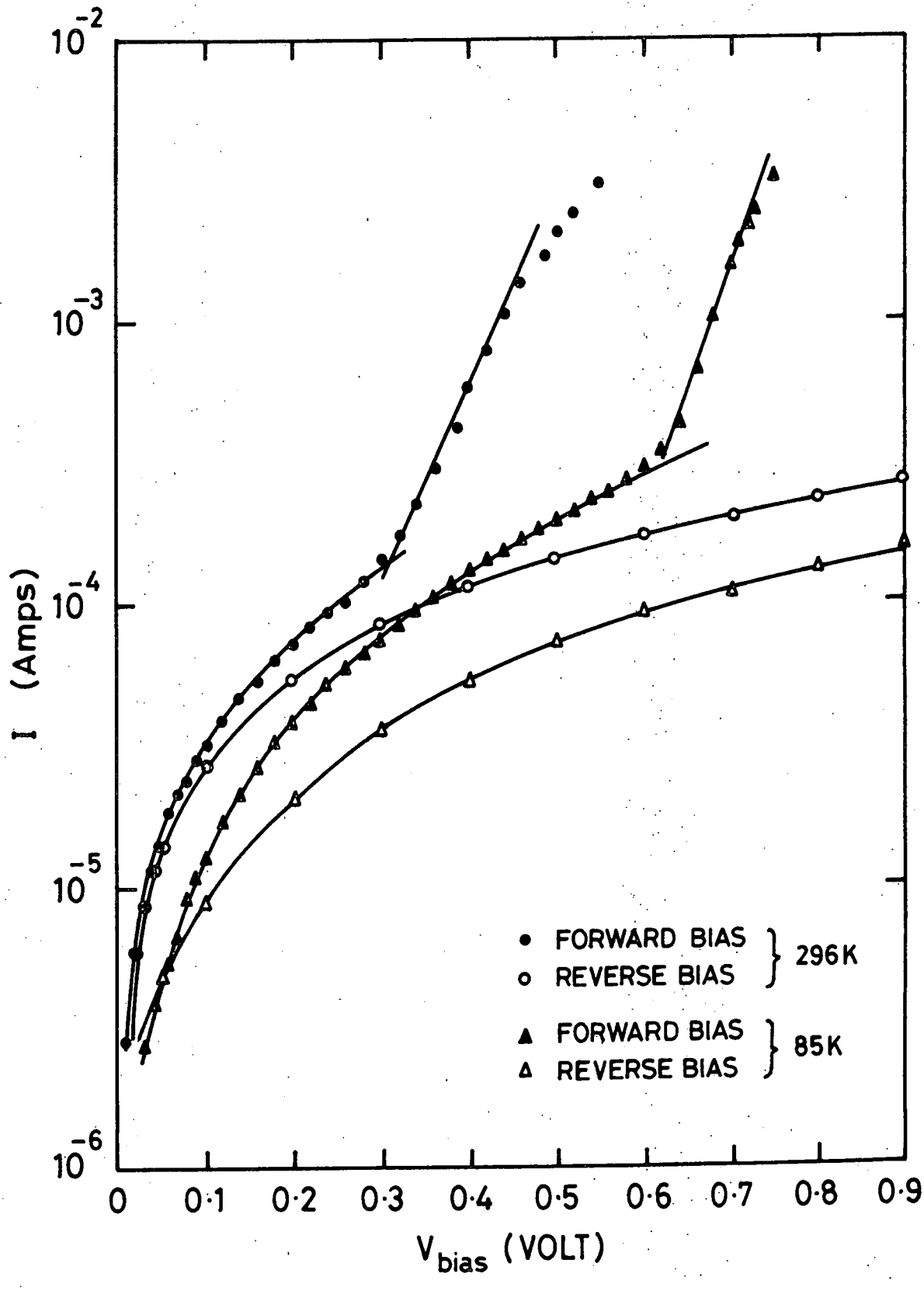

FIG. A·5 DARK CURRENT - VOLTAGE CHARACTERISTICS FOR A GOOD Au - CdS SCHOTTKY BARRIER DIODE MEASURED AT 296 K AND 85 K.

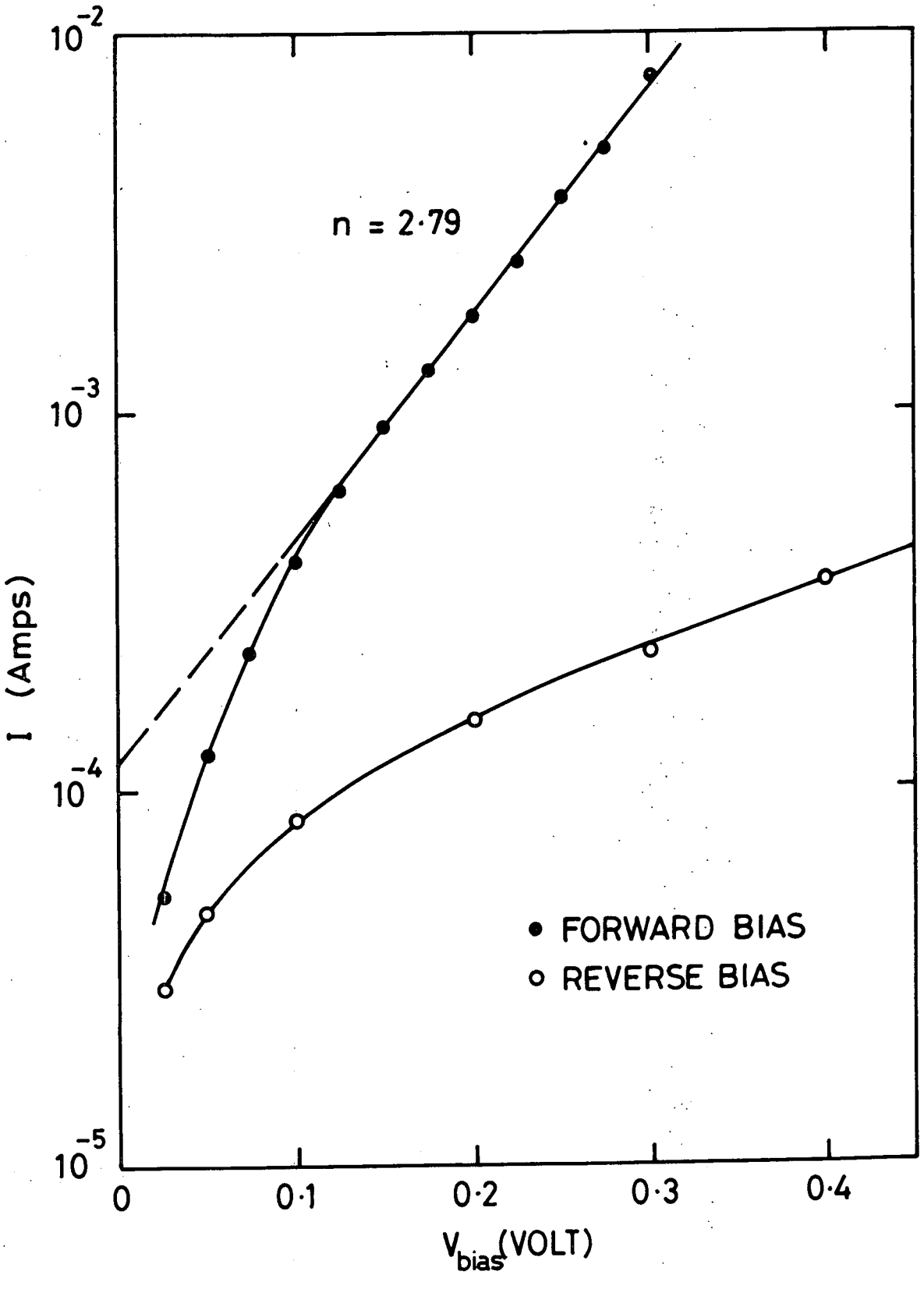

FIG. A·6 DARK CURRENT - VOLTAGE CHARACTERISTICS FOR A POOR Au - CdS SCHOTTKY BARRIER DIODE MEASURED AT 296 K.

Because the Schottky barriers investigated here were fabricated on etched surfaces, it is most likely that interfacial layers were present between the CdS and the metal. It is obvious that the thickness of this interfacial layer will affect the magnitude of the intercept in the C^{-2} - V plot. The discussion on the relation between surface features and the interface state density of the CdS/Cu_2S heterojunction can be extended to the Au-CdS structures to suggest that MS junctions on etched surfaces with hillocks containing many kink sites and ledges will have a high density of interface states. Such a high density of interface states could lock the top of the barrier relative to the Fermi level[4] and thus modify the barrier height and ideality factor. In contrast M-S junctions fabricated on smoothly facetted hillocks will result in relatively low densities of interface states, so that electrons surmounting the potential barrier will tunnel through the interfacial layer. In practice both mechanisms are operative for forward current conduction but the dominant process is determined by the density of the interface states.

REFERENCES - APPENDIX

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